PSIA-2722

Programmable Serial Interface Adapter

USER'S MANUAL

Audio precision®

PSIA-2722
User's Manual

Installation and Operation of the Audio Precision Programmable Serial Interface Adapter

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Contents

Safety Information

Do NOT service or repair this product unless properly qualified. Servicing should be performed only by a qualified technician or an authorized Audio Precision distributor.

One of two external power supplies is provided with this product:

The power supply PN 4540.0020 is designed to operate only from an AC power source (100 V–240 V rms, 47 Hz–63 Hz) with an approved three-conductor power cord and safety grounding. Do NOT defeat the safety ground connection.

The power supply PN 4540.0051 is designed to operate only from an AC power source (100 V–240 V rms, 50 Hz–60 Hz). This power supply has an integral 2-conductor mains plug.

Either power supply automatically adjusts to the line voltage and frequency within the specified range. No user adjustments are necessary. Neither of the power supplies nor the PSIA-2722 contain user-replaceable fuses.

Use only the AP power supply PN 4540.0020 or PN 4540.0051 with the PSIA-2722. The use of other power supplies may result in damage to the PSIA-2722, electrical shock hazard from the power supply or the PSIA-2722, and loss of fire hazard protection.

This product and power supply are for indoor use ONLY.

Safety Symbols

The following symbols may be marked on the panels or covers of equipment or modules, and may be used in this manual:

WARNING!—This symbol alerts you to a potentially hazardous condition, such as the presence of dangerous voltage that could pose a risk of electrical shock. Refer to the accompanying Warning Label or Tag, and exercise extreme caution.

ATTENTION!—This symbol alerts you to important operating considerations or a potential operating condition that could damage equipment. If you see this marked on equipment, consult the User's Manual or Operator's Manual for precautionary instructions.

FUNCTIONAL EARTH TERMINAL—This symbol marks a terminal that is electrically connected to a reference point of a measuring circuit or output and is intended to be earthed for any functional purpose other than safety.

PROTECTIVE EARTH TERMINAL—This symbol marks a terminal that is bonded to conductive parts of the instrument. Confirm that this terminal is connected to an external protective earthing system.

Chapter 1

Introduction

Figure 1. The Audio Precision PSIA-2722 Programmable Serial Interface Adapter.

The PSIA-2722 Programmable Serial Interface Adapter is an accessory unit for Audio Precision's System Two Cascade, Cascade *Plus* and 2700 Series digitally-capable instruments. Since the PSIA operations for all these systems are identical, in this manual the designation "instrument" indicates any of the above models.

When used without a serial interface adapter, the instrument can provide AES3 and IEC60958 serial digital inputs and outputs at a wide range of sample rates and resolutions, as well as parallel digital inputs and outputs. A serial interface adapter such as PSIA-2722, however, is required to transmit or receive digital signals and associated clock inputs and outputs for non-AES3/IEC60958 serial formats often encountered in telecommunications and converter design and testing.

The PSIA-2722 is similar in capability to the earlier Audio Precision SIA-2322, with a key difference: the PSIA-2722 is software controlled. Where configuring the SIA-2322 involved the manual setting of a number of DIP switches for each test setup, PSIA-2722 is configured from the PSIA panel in the instrument control software. The setting of master clock rate, N*Fs clock rate, bit rate, number of channels, word length and sample rate is more intuitive and is aided by automatic calculations. Each test configuration is now

saved as part of the instrument test file. Setups for specific converters can be loaded from previous tests or imported from sample files.

The PSIA-2722 must be connected to an Audio Precision instrument running the appropriate control software:

- For System Two Cascade and System Two Cascade *Plus* instruments, the control software must be APWIN version 2.22 or 2.24, or AP2700. We strongly recommend AP2700 version 3.10.
- For a 2700 Series instrument, the control software must be AP2700.We strongly recommend AP2700 version 3.10.

AP2700 control software is available by download from the Audio Precision Web site at audioprecision.com.

The instrument parallel digital output and input provide data connections for the PSIA; additional cables connect the instrument master clock and the APIB control bus to the PSIA-2722. The PSIA is powered by a separate 5 VDC power supply.

The PSIA provides all necessary serial input, output and clock ports for device connection, as well as provision for oscilloscope monitoring of the various signals. The voltage levels of all the PSIA ports can be set to accommodate devices from different logic families.

Capabilities

Transmitter and Receiver

PSIA-2722 has a serial transmitter section for testing devices with digital input, such as DACs; and a serial receiver section for testing devices with digital output, such as ADCs. Each section is configurable to a wide range of clock and data settings, using either internal or external clock references.

The transmitter and receiver sections can also be operated simultaneously for SRC or other testing. When the instrument's internal master clock is used as the only clock in this configuration, the clock rates of the two sections are tightly coupled. When this configuration is used with a second, external master clock (typical of SRC testing), the controls and functions of the transmitter and receiver are almost entirely independent.

Data and Clock ports

The transmitter and receiver sections each have ports and software panel controls for

- Data
- Frame Clock

- Channel Clock
- Bit Clock
- N*Fs Clock
- Master Clock

Within certain constraints, the clocks can be set to a wide selection of rates. For SRC testing, transmitter and receiver clocks can be set to different rates when a second master clock frequency is provided. Configuration of clock signal polarity, edge sync, pulse width and sync relation to data is available where appropriate.

The Master Clock, Bit Clock and Frame Clock ports can be configured as inputs or outputs, enabling independent selection of master or slave mode for receiver and transmitter.

Data settings

For transmission, the data are provided from the instrument as determined by the Digital Generator and Digital I/O settings, and the PSIA configures this data in a serial stream for the device under test (DUT).

For reception, the serial stream comes from the DUT, and the PSIA must be set to match the incoming data configuration.

The arrangement of the data within the serial word can be set or matched by adjusting four parameters:

- The data length in bits,
- The padding bits before and after the data (if any),
- The state of the padding bits,
- The order of the data bits (MSB or LSB first).

Also, the timing relationship between the data and the bit clock (synchronized on the rising or falling edge) can be set.

Voltage levels

PSIA clock and data ports can be set to interface with common logic families:

- 5.0 V TTL
- 3.3 V TTL
- 3.3 V CMOS
- 2.4 V CMOS
- 1.8 V CMOS

Documentation

This *PSIA-2722 User's Manual* is the primary document for the PSIA. Converter testing also requires a good understanding of many of the functions of the Audio Precision instrument; these are covered in detail in the instrument's *User's Manual*.

Context-sensitive Help information for the PSIA is included within the control software.

Visit the Audio Precision Web site at audioprecision.com for more information on using the PSIA.

Chapter 2

Installation and Setup

Figure 2. PSIA-2722 and a System Two Cascade Plus.

The PSIA-2722 is an accessory to Audio Precision's System Two Cascade, Cascade *Plus* and 2700 Series digitally-capable instruments. Since the PSIA operations for all these systems are identical, in this manual the designation "instrument" indicates any of the above models.

The PSIA-2722 must be connected to an Audio Precision instrument running the appropriate control software:

- For System Two Cascade and System Two Cascade *Plus* instruments, the control software must be APWIN version 2.22 or 2.24, or AP2700. We strongly recommend AP2700 version 3.10.
- For a 2700 Series instrument, the control software must be AP2700.We strongly recommend AP2700 version 3.10.

AP2700 control software is available by download from the Audio Precision Web site at audioprecision.com.

See your instrument *Getting Started* manual for information on setting up your Audio Precision instrument.

PSIA-2722 Components

When you open the shipping box you will find:

- The PSIA-2722 chassis.
- A 5 VDC external universal mains power supply, selected for your location; either PN 4540.0020 or PN 4540.0051. The power supply output cord is attached to the PSIA-2722 chassis.
- If your power supply is PN 4540.0020, there will be a mains cable for the power supply. Power supply PN 4540.0051 has an integral mains plug.
- An APIB cable. This cable is for exchange of control data between the PSIA, the instrument and the controlling PC.
- Two 25-wire parallel digital cables. These are used for digital data communications between the PSIA and the instrument.
- Four 50 Ω coax cables each fitted with BNC connectors on both ends. These are used for instrument Master Clock connection and for "Loop-Back" testing.
- Two cable harnesses, each of six 50 Ω coax cables fitted with BNC connectors on one end and dual square pin connectors on the other. These are used for connection to the DUT.
- This manual.

Power Supply

Use only the power supply provided by Audio Precision (AP part number 4540.0020 or 4540.0051) for powering the PSIA. There is no user-replaceable fuse for either power supply.

PN 4540.0020

The PN 4540.0020 DC power supply accommodates mains voltages from 100 VAC to 240 VAC and mains frequencies from 47 Hz to 63 Hz. Maximum current consumption is 0.4 A.

If the power supply ON indicator (a green LED near the AP label) does not light when AC mains power is applied to the DC power supply, verify that the

mains power cord is functioning properly. If the ON indicator still does not light, contact Audio Precision for a replacement supply.

PN 4540.0051

The PN 4540.0051 DC power supply accommodates mains voltages from 100 VAC to 240 VAC and mains frequencies from 50 Hz to 60 Hz. Maximum current consumption is 1.0 A.

Connecting the PSIA to the instrument

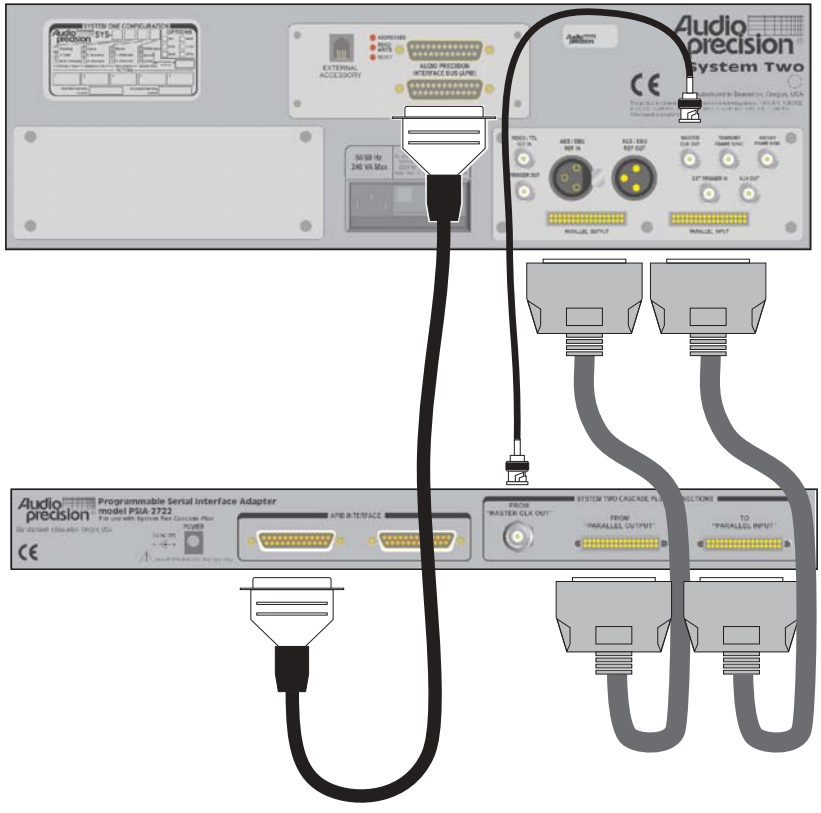


Figure 3. PSIA-2722-to-instrument rear-panel system interconnections.

Place the PSIA near both the instrument and the device that you want to test. Using an APIB cable, connect the instrument to a PC that has AP2700 (or APWIN version 2.22 or 2.24) installed.

Be sure the mains power is OFF for both the instrument and the PSIA. Then connect the four cables between the instrument and the PSIA following these instructions. See Figure 3.

- Attach the APIB cable from one of the PSIA **APIB** connectors to the unused **APIB** connector on the instrument rear panel.
- Connect a 50 Ω BNC cable from the instrument **MASTER CLOCK OUT** BNC connector to the PSIA rear-panel jack labeled **FROM MASTER CLK OUT**.
- Connect one 25-wire parallel digital cable from the instrument **PARALLEL OUTPUT** to the PSIA connector labeled **FROM PARALLEL OUTPUT**.
- Connect the second 25-wire parallel digital cable from the instrument **PARALLEL INPUT** to the PSIA connector labeled **TO PARALLEL INPUT**.

Finally, insert the 5.5 mm coaxial plug from the 5 VDC power supply into the **POWER** jack on the rear of the PSIA, and plug the mains power cord into the electrical mains supply. This will power up the PSIA and light the **OUT/IN** and **LOGIC VOLTAGE SUPPLY** LEDs.

Switch the instrument ON and launch the control software.

If an APIB cable is connected between the instrument and the PSIA but the PSIA is not powered ON, the control software will start in Demo Mode. Be sure that the PSIA is ON when starting the control software with the APIB cable connected.

If you connect the PSIA to the instrument after the control software has been launched, choose **Utilities > Restore Hardware** to enable the software to recognize the presence of the PSIA.

All four instrument-to-PSIA cables must be connected for the PSIA to operate properly.

Chapter 3

Converter Testing

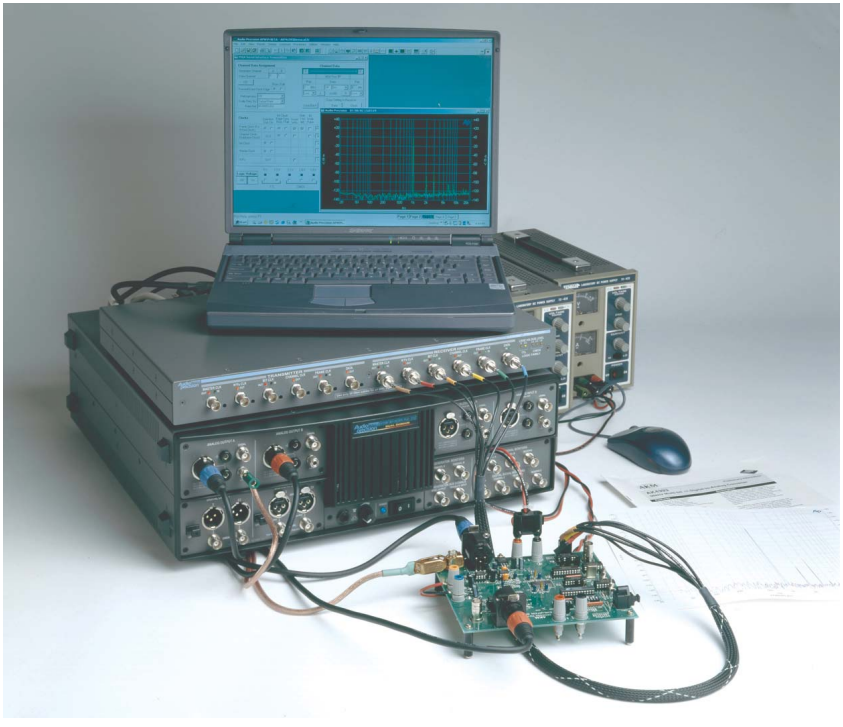


Figure 4. PSIA-2722 with Audio Precision instrument and coverter test fixture.

PSIA-2722 is designed to enable testing of audio analog-to-digital converters (ADCs), digital-to-analog converters (DACs) and other digital devices that have data or clock characteristics that are not compatible with the AES3 / IEC60958 (also called AES/EBU and SPDIF) digital serial interface standards.

The AES3 and IEC60958 standards limit the audio data word length and format, number of channels, sample rates, and sychronization relationships to

a narrow range of choices. These standards also specify the addition of metadata and the superimposition of clock rate and data into one stream by use of bi-phase mark encoding.

The PSIA transmitter and receiver are unconstrained by these standards. Each section has five clock ports and one data port, enabling common three- or four-wire serial interfacing. Each section can be operated in a master or slave relationship with the DUT. Clock relationships and clock-to-data relationships are variable, and with an additional master clock generator the transmitter and receiver sections can be set to different sample rates for SRC testing.

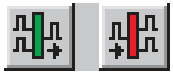
This chapter provides an overview of digital converter testing with an Audio Precision instrument and the PSIA-2722, including connection diagrams and PSIA software panel operation. Examples of actual converter setups are detailed on the Audio Precision Web site. See Appendix B for more information about test configuration examples and sample files.

Relationship between PSIA and the instrument

The PSIA-2722 has no function without an Audio Precision instrument. All signal generation and analysis, DSP processing, and computer control operations such as file handling, data display, etc., are performed by the instrument.

The instrument digital or analog audio generators and analyzers selected for a particular test will be used with the PSIA in the same way that they would be in testing using the AES3 interface, but PSIA functions replace the instrument's internal AES3 transmitter/receiver.

See Chapter 2 for information on interconnecting the instrument hardware with the PSIA.



The control software provides two PSIA software panels for serial interface operation. Click on the PSIA **Transmitter** (green) or PSIA **Receiver** (red) buttons on the Toolbar, or choose **Panels > PSIA Transmitter** or **Panels > PSIA Receiver** on the Main menu or press **Ctrl-T** or **Ctrl-R** to open the panels.

Next open the DIO panel by clicking the DIO button or by choosing **Panels > Digital Input/Output**. Enable PSIA operation for input or output by selecting **PSIA** as the DIO **Input: Connector** or **Output: Connector** (APWIN: **Input: Format** or **Output: Format**) setting.

A number of DIO panel controls and displays also affect the PSIA; for convenience, some of these controls and displays are duplicated on the PSIA panels. See **Duplicated Displays and Controls** on page 19.

PSIA Transmitter and Receiver Connections

Figure 6. The PSIA-2722 front panel.

The PSIA-2722 communicates with the device under test through its front-panel Transmitter and Receiver ports.

Use the six-cable harnesses provided to connect the PSIA transmitter or receiver to the DUT. If your DUT has BNC connectors rather than square pin connectors, use high-quality 50 Ω coaxial BNC cables of matched length. Connection diagrams for Loop-Back, ADC testing, DAC testing and SRC testing configurations follow.

Connect an oscilloscope

It is useful to view the clock and data waveforms simultaneously on a multi-channel oscilloscope while configuring and testing the PSIA. Dedicated scope monitoring jacks are provided for each PSIA port. See **Oscilloscope Monitoring** on page 46.

Connections for Loop-Back configuration

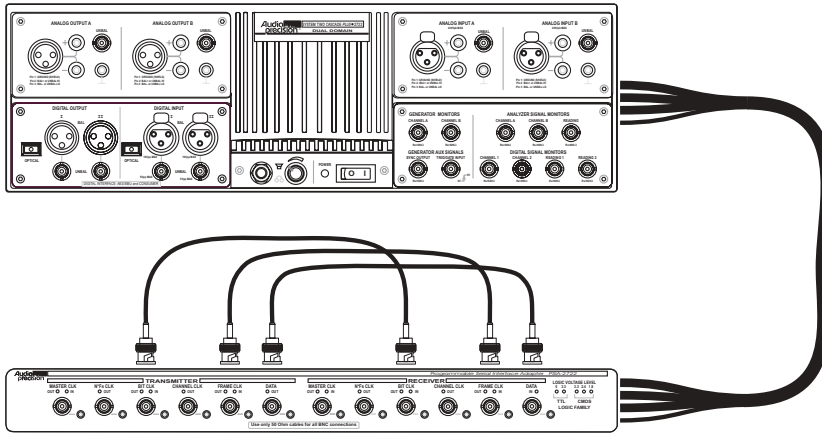


Figure 5. PSIA-2722 in Loop-Back configuration.

Begin each new setup by running a test with the PSIA in a Loop-Back configuration, which requires the use of both the PSIA Transmitter and Receiver sections. Running a test in Loop-Back configuration is a simple way of verifying that your PSIA Transmitter and Receiver settings are compatible, that syn-

chronization and data signals are passing properly through the PSIA, and that the instrument Generator, Analyzer, DIO settings and test parameters are appropriate for PSIA use. Set up a Loop-Back test by following these steps:

- On the DIO panel, choose **PSIA** in both the **Input: Connector** (APWIN: **Input: Format**) list and the **Output: Connector** (APWIN: **Output: Format**) list. This will enable both Transmitter and Receiver panels.
- Open both the PSIA Transmitter and Receiver panels.
- Connect three loop-back cables between the PSIA Transmitter and Receiver Bit Clock, Frame Clock and Data ports. See Figure 5.
- Run a simple test through the PSIA loop-back. This will verify that the PSIA is connected correctly and that your test is compatible and properly configured.
  A typical "simple test" might be a 1 kHz sine wave from the Digital Generator routed to the PSIA via the DIO Output setting, then brought back into the instrument from the PSIA via the DIO Input setting and routed into the FFT analyzer where a frequency-domain graph is created.

  *In a **New Test,** the PSIA Transmitter and Receiver sections have compatible settings by default, ready for a loop-back test.*

- With the loop-back cables connected, re-set the PSIA controls for the data configuration, clock rates and logic voltages required for testing your DUT. Run your test again to verify that the test is still compatible and properly configured for these new settings.

Connections for ADC testing

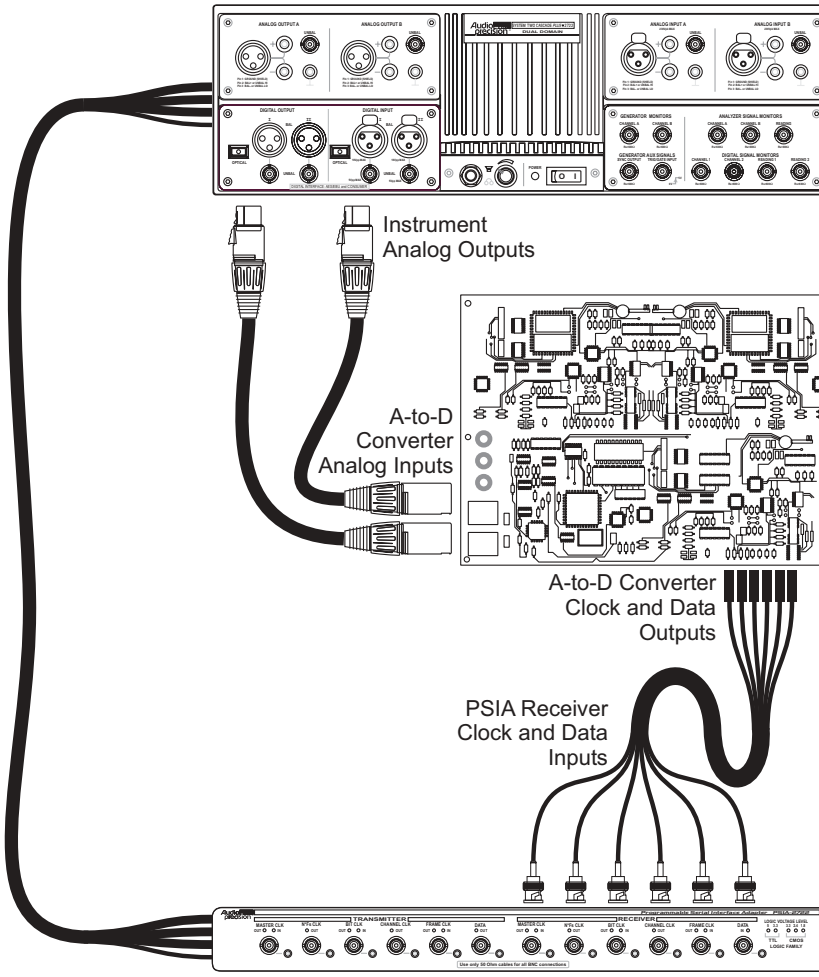


Figure 7. ADC testing with the PSIA-2722.

First, set the PSIA LOGIC VOLTAGE LEVEL (see page 33) to the correct voltage setting for the logic circuits in the ADC.

For analog-to-digital converter (ADC) testing, the instrument provides stimulus signals directly to the ADC in the analog domain and analyzes the device output in the digital domain via the PSIA receiver and the instrument's DIO.

Set any jumpers or switches necessary for the test on your DUT. Connect your DUT to the proper PSIA ports and make any other direct audio or digital connection from the DUT to the instrument necessary for your test, as shown in Figure 7. Many device tests will not require all the available PSIA connec-

tions. In most cases, only the Data, Frame Clock and Bit Clock connections are necessary.

Make your generator and analyzer settings compatible with the characteristics of your device.

Apply power to the DUT.

Connections for DAC testing

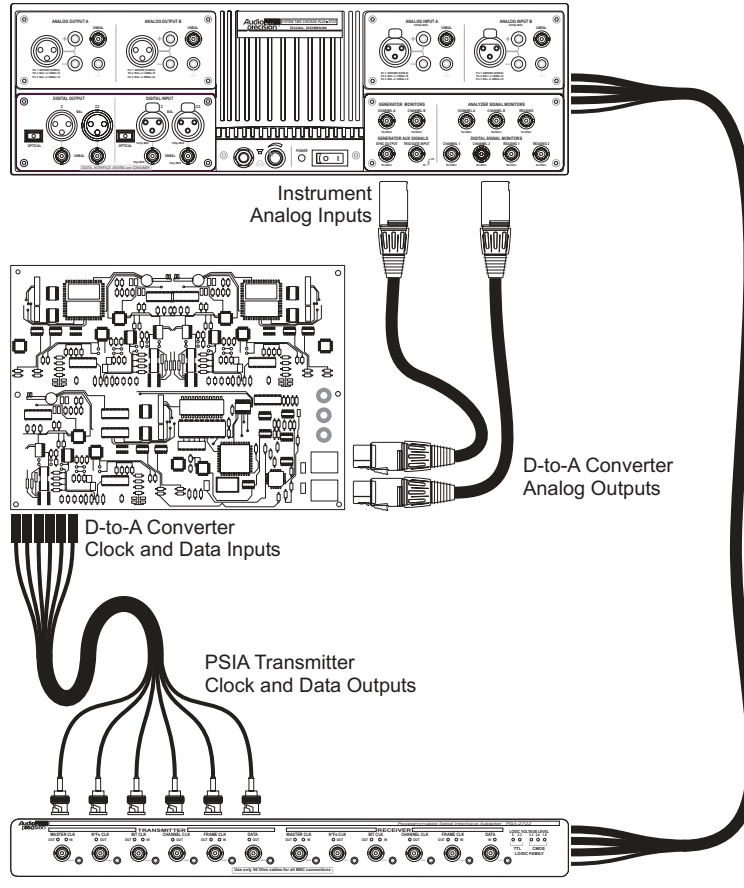


Figure 8. DAC testing with the PSIA-2722.

First, set the PSIA LOGIC VOLTAGE LEVEL (see page 33) to the correct voltage setting for the logic circuits in the DAC.

For digital-to-analog converter (DAC) testing, the instrument provides stimulus signals in the digital domain via the DIO and the PSIA Transmitter, and directly analyzes the device output in the analog domain.

Only the PSIA Transmitter panel is needed for DAC testing, and the PSIA Receiver panel may be closed. If you have another use for the DIO Input, you may de-select **PSIA** in the **Input: Connector** (APWIN: **Input: Format**) list.

Set any jumpers or switches necessary for the test on your DUT. Connect your device to the proper PSIA ports and make any other direct audio or digital connection from the DUT to the instrument that is necessary for your test, as shown in Figure 8. Many device tests will not require all the available PSIA connections. In most cases, only the Data, Frame Clock and Bit Clock connections are necessary.

Make your generator and analyzer settings compatible with the characteristics of your device.

Apply power to the DUT.

Connections for SRC testing

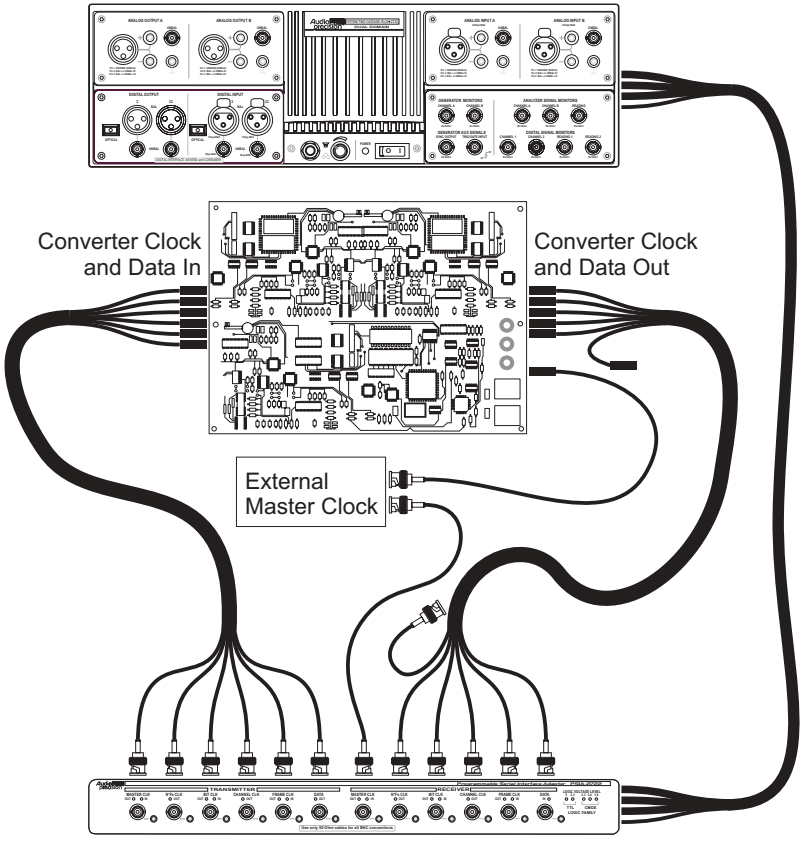


Figure 9. SRC testing with the PSIA-2722.

First, set the PSIA LOGIC VOLTAGE LEVEL (see page 33) to the correct voltage setting for the logic circuits in the SRC.

A sample rate converter (SRC) has digital inputs and outputs and does not require analog generation or analysis capability. For SRC testing, the instrument provides stimulus signals in the digital domain via the DIO and the PSIA Transmitter, and analyzes the device output in the digital domain via the PSIA receiver and the DIO.

For SRC and Loop-Back testing, both the PSIA Transmitter and Receiver panels are necessary. You will need to keep **PSIA** as the selection in both the DIO **Input: Connector** and **Output: Connector** (APWIN: **Input: Format** and **Output: Format**) lists.

Set any jumpers or switches necessary for the test on the SRC. Connect the SRC to the proper PSIA ports for your test, as shown in Figure 9. Many device tests will not require all the available PSIA connections. In most cases, only the Data, Frame Clock and Bit Clock connections are necessary.

In SRC testing the PSIA Transmitter and Receiver may be set to sample rates that are not the same: the transmitter may be required to operate at 48 kHz, for example, while the receiver must be set to 44.1 kHz. When using only the instrument/PSIA master clock, dual sample rates are constrained to certain ranges and ratios. For other combinations of sample rate, a second external master clock must be used.

Make your generator and analyzer settings compatible with the characteristics of your device.

Apply power to the DUT.

The Transmitter and Receiver panels

The PSIA Transmitter and Receiver panels are very similar. Figures 10 and 11 show the two panels. The settings and displays are discussed below as they apply to both panels, with the exceptions noted.

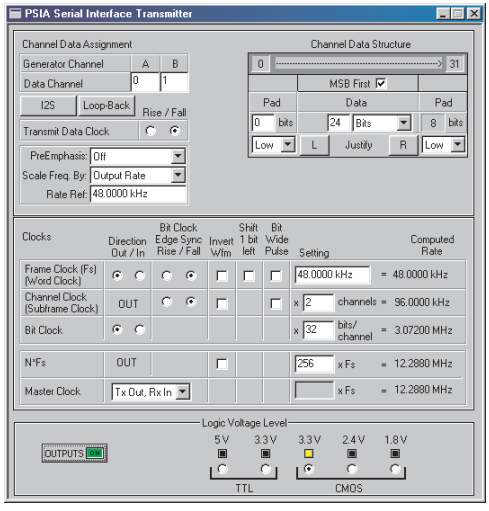
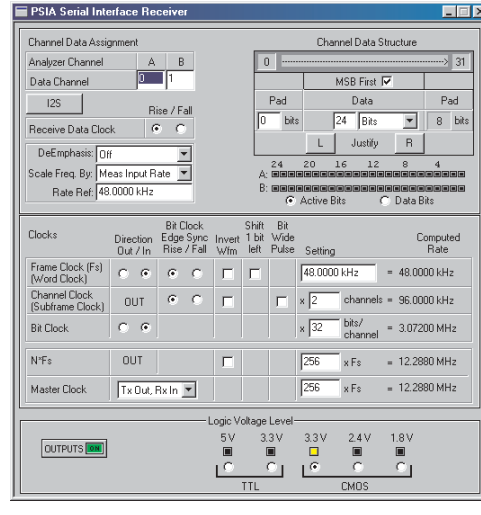


Figure 10. The PSIA Transmitter panel.

Figure 11. The PSIA Receiver panel.



Click on the PSIA **Transmitter** (green) or PSIA **Receiver** (red) buttons on the Toolbar, or choose **Panels > PSIA Transmitter** or **Panels > PSIA Receiver** on the Main Menu to open the panels.

Transmitter and Receiver Settings

The PSIA transmitter embeds the generated audio signal from the instrument in a serial data stream whose characteristics are largely under PSIA control. Similarly, the PSIA receiver has widely variable characteristics to recover the audio signal from a range of device output data streams.

For transmitter and receiver, you can set

- The number of transmitted (received) channels.
- The assignment of the two instrument audio generator (analyzer) channels to the PSIA Transmitter (Receiver) channels.
- The number of bits per channel.
- The number of channel data bits that carry audio.
- The number of channel data bits designated as padding bits.
- The arrangement of the data and padding bits in the word.
- The state of the padding bits.
- The edge sync relationship between the bit clock and the data, frame clock and channel clock signals.
- The rates of several clock signals related to the transmitted output (received input).
- The source of several of the clock signals.
- The synchronization relationship between some of the clock signals, such as setting clock signal polarity, edge sync relationship, duty cycle and “shift left” setting.

For convenience, I^2S (see page 20) settings can me made with one click, and compatible settings can be copied from the Transmitter panel to the Receiver panel using the Loop-Back button.

Duplicated Controls and Displays

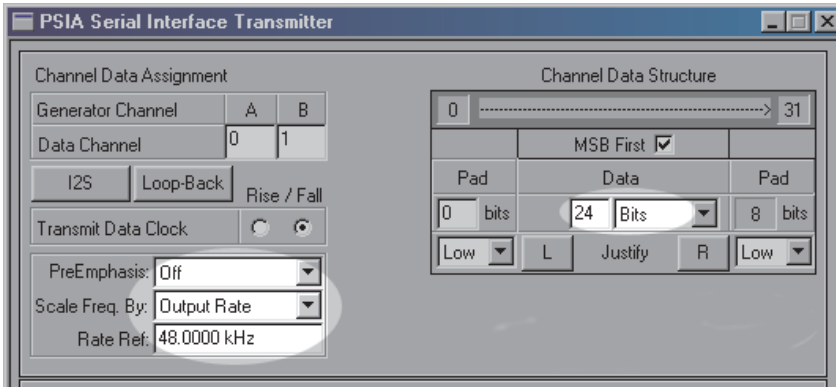


Figure 12. Controls in common between PSIA Transmitter and DIO Output.

Some operations in configuring a serial interface involve changing settings on the Digital Input/Output (DIO) panel. For convenience, controls and displays for the most common of these operations are duplicated on both the DIO panel and on the PSIA panels. Common settings made on one of these panels will be reflected on the others. The figures above and below highlight the duplicated settings and displays.

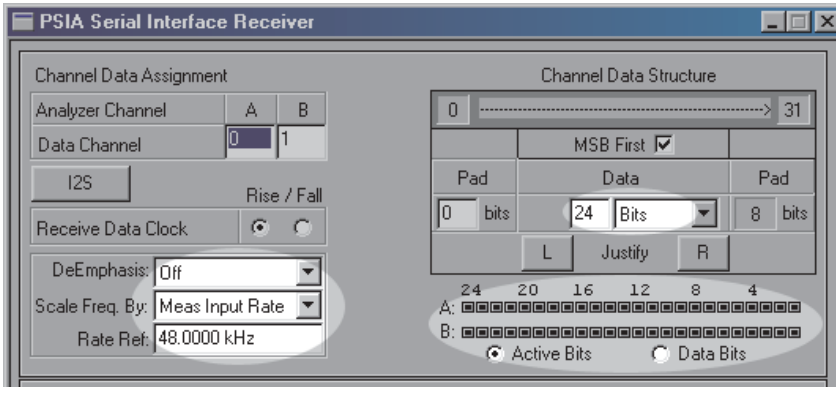
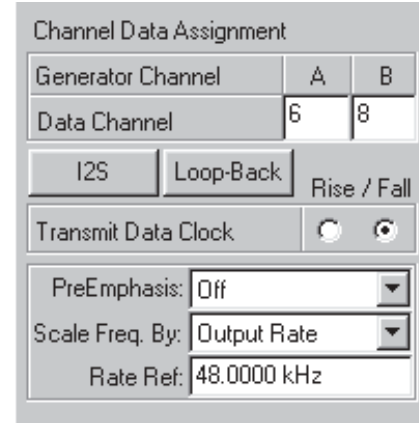


Figure 13. Controls in common with PSIA Receiver and instrument DIO Input.

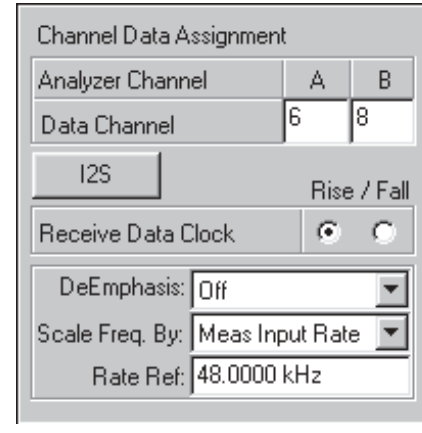
Channel Data Assignment

Figure 14. The PSIA Transmitter Channel Data Assignment and miscellaneous Data settings.



The instrument has two audio channels, **A** and **B**. When the serial interface has more than two channels, you must assign the instrument channels to the interface channels under test. See Figures 14 and 15.

Figure 15. The PSIA Receiver Channel Data Assignment and miscellaneous Data settings.



*To set the number of channels for the serial interface, go to the **Channels** field in the **Setting** column of the Clocks matrix on the Transmitter or Receiver panel. See page 33.*

One-click I²S bus settings

The PSIA **I²S** button provides a one-click method to conform the Transmitter or Receiver settings to the Philips I²S (Inter-IC Sound) standard. See Figure 14.

Specifically, the **I²S** button

- Sets the Channel Data Assignment **A=0**, **B=1**.
- Sets **MSB First**.
- Sets the leading Pad to **0** bits (left justified).
- Sets both Transmitter pad state controls to **Low**.
- Sets the Frame Clock waveform polarity to **Invert Wfm**.
- Sets the Frame Clock / Data relationship to **Shift 1 bit left**.
- Sets the Data clock edge sync to **Fall** for the Transmitter, **Rise** for the Receiver.
- Sets the Frame Clock edge sync to **Fall** if the Frame Clock Direction is set to **Out**, or to **Rise** if the Direction is set to **In**.
- Clears the Frame Clock Bit Wide Pulse checkbox if it was checked.
- Sets the number of channels per frame to **2**.

*Note that parameters set by clicking the **I²S** button are not "locked" to I²S settings; any of these parameters can be reset at any time. The I²S button does not set a defined mode for the PSIA, but is a convenient way to make several settings at once.*

Transmit Data Clock Edge

See Figures 14 and 15. This control establishes whether the leading edges of the Data transitions are aligned with the rising edge or the falling edge of the Bit Clock transitions, as shown in Figure 16. Data pulse edge sync can be set independently for Transmitter and Receiver.

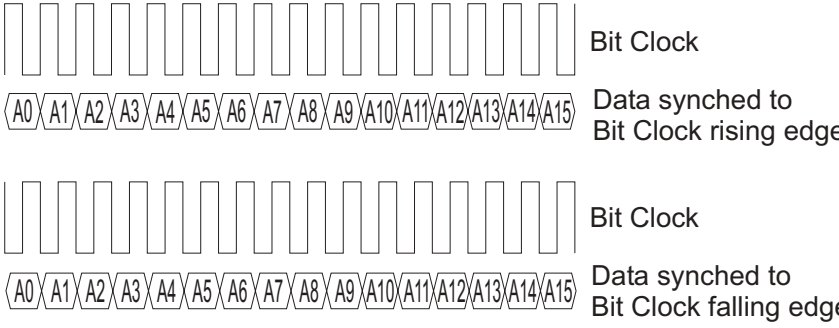


Figure 16. Data sync relationship to Bit Clock edges.

PreEmphasis (Transmitter only)

See Figure 14. This control is a duplicate of the DIO Output **PreEmphasis** control, and enables you to select a preemphasis curve to apply to the embedded audio signal before transmission. Preemphasis for digital audio signals is discussed in more detail in the instrument *User's Manual*.

DeEmphasis (Receiver only)

See Figure 15. This control is a duplicate of the DIO Input **DeEmphasis** control, and enables you to select a deemphasis curve to apply to the embedded audio signal after reception. Deemphasis of digital audio signals is discussed in more detail in the instrument *User's Manual*.

Scale Freq. by

See Figures 14 and 15. This control is a duplicate of the DIO Output **Scale Freq. by** control. It enables you to select the reference by which to scale the audio embedded in the digital signal. Audio frequency scaling for digital signals is discussed below and in the instrument *User's Manual*.

Audio frequency scaling

An embedded audio signal of a particular frequency (1 kHz, for example) will be shifted in frequency if the sample rate at which it is recovered is different from the rate at which it was sampled. The frequency is shifted by the ratio of the two sample rates. In PSIA applications this can occur in SRC or cascaded converter testing.

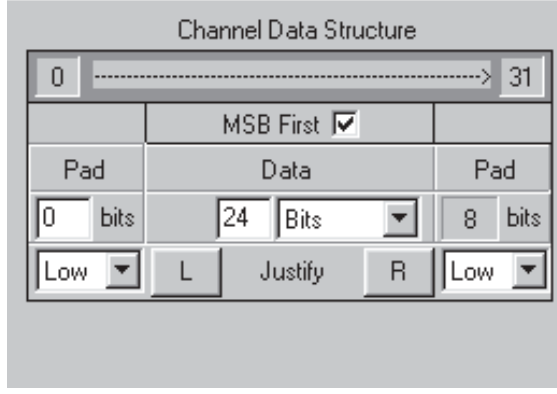
To counteract this frequency shifting, the instrument allows you to scale the audio frequency at transmission or reception. The Output and Input **Scale Freq. By** controls allow you to select one of several sample rate sources as a scaling factor, normalizing the audio frequency.

Rate Ref

See Figures 14 and 15. This control is a duplicate of the DIO Output **Rate Ref** entry field. **Rate Ref** enables you to specify a reference frequency by which to scale the embedded audio frequency before transmission. Audio frequency scaling for digital signals is discussed above and in the instrument *User's Manual*.

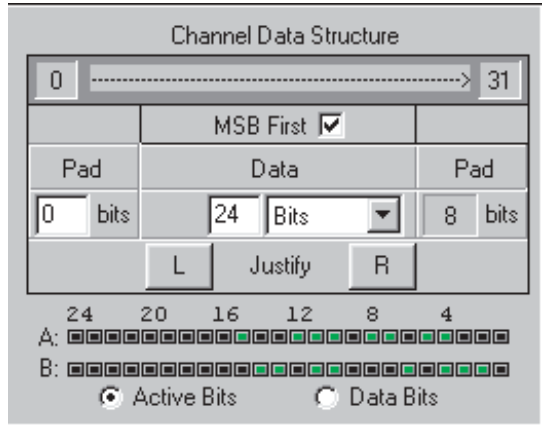
Channel Data

Figure 17. The PSIA Transmitter Channel Data configuration settings.



See Figures 17 and 18. This section of the panel enables you to define the characteristics of the channel data: word length, data padding, data direction and so on. The two data **Resolution** fields (displaying **24** and **Bits** in Figure 18) are shared with the DIO; the other fields only affect PSIA operation.

Figure 18. The PSIA Receiver Channel Data configuration settings.



Many of these controls are interrelated with other controls on the PSIA transmitter panel.

Bits per channel display

The top line of this display shows the number of bits per channel, set below in the Clocks matrix. 32 bits per channel, for example, is shown as 0------->31, as in Figures 17 and 18.

*To set the number of channels for the serial interface, go to the **Channels** field in the **Setting** column of the Clocks matrix on the Transmitter or Receiver panel. See page 33.*

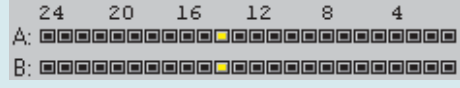
MSB first: Transmitter

When the **MSB First** box is checked, the MSB (most significant bit) of the data is sent first. When the box is not checked, the LSB (least significant bit) is sent first. See Figures 17 and 18.

MSB first: Receiver

When the **MSB First** box is checked, the first bit of data received is considered to be the MSB (most significant bit). When the box is not checked, the first received bit is considered to be the LSB (least significant bit). See Figures 17 and 18.

Walking Ones



*Running the **Special: Walking Ones** waveform is an easy way to observe the MSB-first or LSB-first configuration. On the Receiver / DIO Data bits display, or on an oscilloscope, the "walking one" bit will move from right to left when the PSIA is set to MSB First. The bit will walk from left to right when the PSIA Transmitter is changed to LSB first.*

*On the **Special: Walking Ones** waveform panel, set **Samples/Step** to the same value as **Fs**. This will cause the bit to "walk" at a rate of one step per second.*

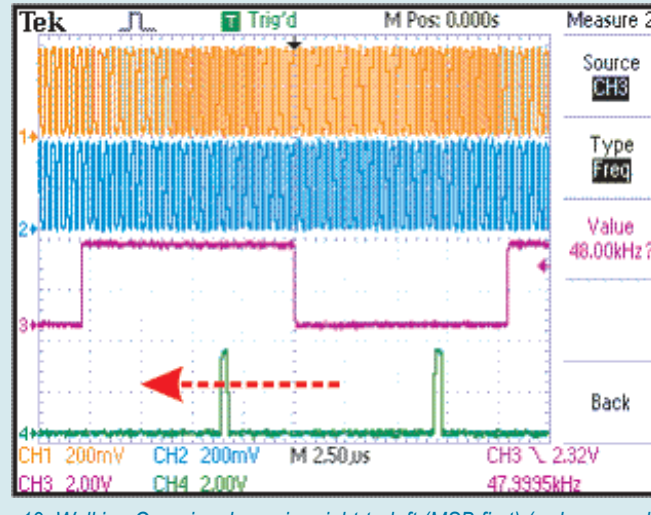


Figure 19. Walking One signal, moving right-to-left (MSB first) (red arrow added).

Data and padding controls

See Figures 17 and 18. In some serial interface signals, the entire bit allocation for the channel carries audio information. In other configurations, only some of the bits carry audio. The remaining bits are called *pads* or *padding bits,* and they can be placed before, after, or before and after the audio bits. The padding bits can also be set to specific logic states.

The Data and Pad controls enable you to set all these parameters, or to set the Data to linear PCM or to µ-Law, A-Law or the IEC61937 protocols. (The OPT-2711 Dolby Digital option must be installed in the instrument for IEC61937 operation).

Data

See Figures 17 and 18.

As mentioned above, the number of bits in the channel is set in the **Channels** field in the **Setting** column of the Clocks matrix on the Transmitter or Receiver panel. See page 33.

The number of active audio bits in the channel is set in the left **Data** field here. This control is a duplicate of the Output resolution field (for the transmitter; for the receiver, Input resolution) on the DIO panel.

Enter the number of active bits in the left field. Integers from **8** to **24** are valid. The sum of the pad bits and the data bits cannot exceed the total channel bits.

The right Data field is normally set to **Linear** (APWIN: **Bits**). The drop-down list also allows you to select µ-Law, A-Law or IEC61937. This control is a duplicate of the second Output resolution field (for the transmitter; for the receiver, Input resolution) on the DIO panel. (The OPT-2711 Dolby Digital option must be installed in the instrument for IEC61937 operation).

Pads

See Figures 17 and 18.

Whenever the active data bits are fewer than the number of channel bits, padding bits must fill out the channel. The sum of the leading pad bits, the audio bits and the trailing pad bits always equals the total number of bits per channel.

If the leading (left) **Pad** field is set to fewer than the number of channel bits minus the number of audio bits, the necessary padding bits will be added after the audio bits, and the number of these bits will be displayed in the trailing **Pad** field.

Left and Right Justify: Transmitter

See Figure 17.

You can quickly put all the padding bits to either the trailing or the leading edge with the click of one button. Click the **L Justify** button to set the active bits fully to the left (0 leading pad, all padding bits trailing). Click the **R Justify** button to set the active bits fully right (0 trailing pad, all padding bits leading).

The **Justify** buttons enter values into the leading and trailing **Pad** fields. You can modify these values at any time.

Left and Right Justify: Receiver

See Figure 18.

The **L** and **R Justify** buttons have a complementary function on the Receiver panel, configuring the software to expect a left or right justified data stream. As on the Transmitter panel, the **Justify** buttons enter values into the leading and trailing Pad fields. You can modify these values at any time.

Pad bits logic states (Transmitter only)

These controls are only on the Transmitter panel. See Figure 17.

The drop-down lists below each of the **Pad** fields enable you to set the logic state of the leading and trailing padding bits.

- **Low** sets the padding bits to logical low.
- **High** sets the padding bits to logical high.
- **Nearest Bit** sets the padding bits to the same logical state as the data bit adjacent to the pad. If that bit is the LSB, then the padding bits are set to LSB. If MSB, then the padding bits are MSB (since the MSB is the sign bit, this is also called *sign extension*).

Data Bit Indicators

This display is only on the Receiver panel. See Figure 18.

The **Data Bit** indicators show a bit-by-bit view of the embedded data in the two channels assigned to Analyzer Channel A and Channel B. This display is the same as the Data Bits display on the DIO panel.

The bits are labeled from the left from the most significant bit (MSB, or bit 24 of the word) to the least significant bit (LSB, or bit 1 of the word) on the right. The **Data Bit** indicators examine the signal in intervals of approximately 1/4 second.

The Data Bit indicators have two modes, selectable by the option buttons to the right of the indicator rows.

When **Data Bits** is selected, the indicators display green for a bit that is at data 1 at the moment of measurement, and black for a bit that is at data 0.

When **Active Bits** is selected, the indicators display green for a bit that has changed state during the measurement period, and black for a bit that has not.

The Clocks control matrix

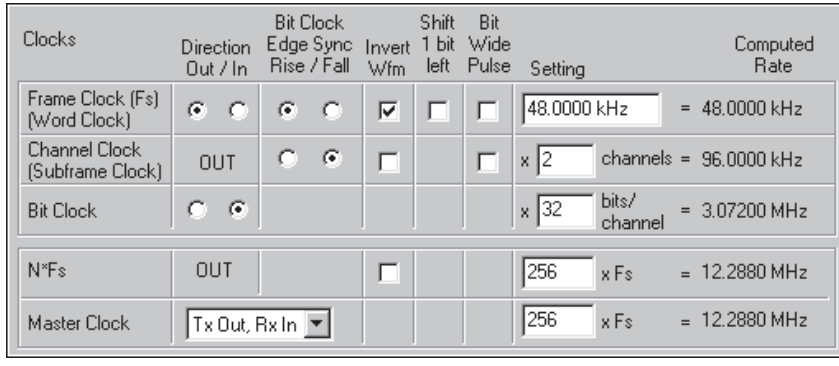


Figure 20. The PSIA Transmitter and Receiver Clocks control matrix.

The clock controls are set into a matrix pattern to illustrate the relationships among the five clock signals and settings that govern them.

The Clock signals

The five clock signals for the PSIA transmitter or receiver are:

- The Frame Clock
- The Channel Clock
- The Bit Clock
- The N*Fs Clock
- The Master Clock

The Clock controls

Several fields enable you to control various aspects of the relationship of each clock with the other clocks. Because of their different functions, each clock signal has a different combination of controls available.

Direction

See Figure 20.

Each of the clock and data ports for both the Transmitter and the Receiver sections of the PSIA has a direction associated with it. A port that is designated as an Output provides a signal from the PSIA to the DUT. A port designated as an Input accepts a signal from the DUT into the PSIA.

Master mode and slave mode

When a PSIA Transmitter or Receiver section has all its clock ports set as Outputs, that section is a master, and the DUT is a slave. When any clock port is set as an Input, the DUT is the master and the PSIA is a slave.

These choices are available for the PSIA ports:

- Master Clock: **Tx IN + Rx IN**, **Tx OUT + Rx IN**, **Tx IN + Rx OUT**
- N*Fs Clock: **OUT**
- Bit Clock: **OUT / IN**
- Channel Clock: **OUT**
- Frame Clock: **OUT / IN**
- Data: **Tx OUT**, **Rx IN**

When the bit clock is set to **IN**, a master clock connection to the DUT is unnecessary. In this case, set the Clock Direction for the unused Master Clock port to **IN**.

Clock direction settings are echoed by red (**OUT**) and green (**IN**) LEDs on the PSIA front panel.

Bit Clock Edge Sync (Frame Clock and Channel Clock)

See Figures 20 and 22.

These controls establish whether the leading edges of the Frame Clock or Channel Clock transitions are aligned with the rising edge or the falling edge of the Bit Clock transitions. Frame Clock and Channel Clock edge sync can be set independently for Transmitter and Receiver.

Invert Waveform (Frame, Channel and N*Fs Clocks)

See Figure 20.

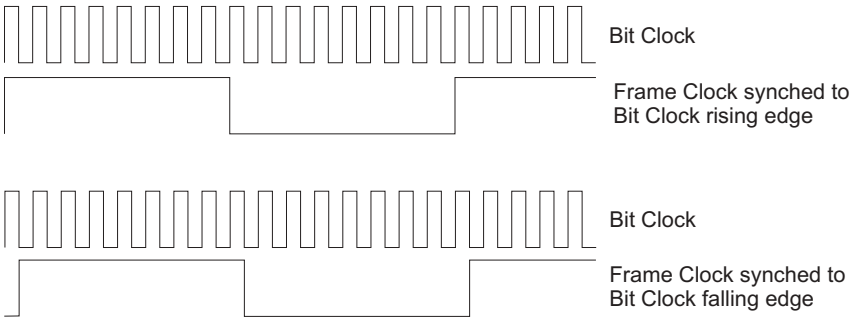


Figure 22. Frame Clock sync relationship to Bit Clock edges.

This control is available for the **Frame Clock,** the **Channel Clock** and the **N*Fs Clock.** The control establishes whether the clock waveform has normal or inverted polarity relative to the bit clock.

Some devices require inverted polarity for a particular clock signal. Clock inversion is also useful to establish synchronization in circumstances in which signal components have undergone different propagation delays.

For example, consider a system in which the data is to align with the rising edge of a clock signal. If either signal has been delayed by more than half the period of the clock signal, it may fall out of the tolerance of the system and lose synchronization. Inverting the clock signal will reduce the relative delay to less than half the period. If this places the offset within the tolerance of the system, sychronization is re-established.

Shift One Bit Left (Frame Clock Only)

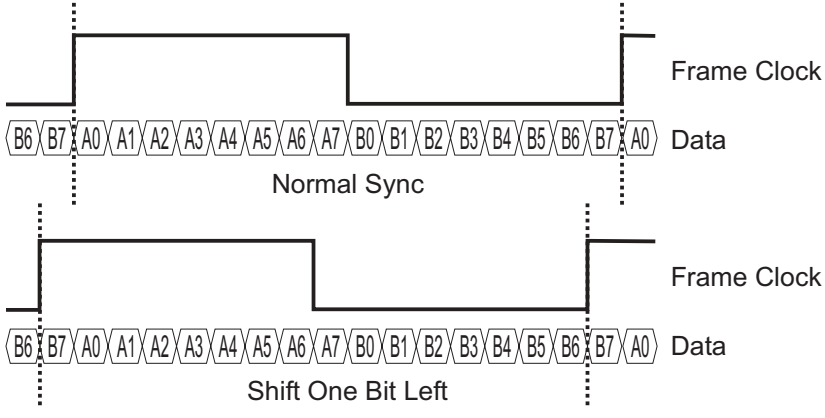


Figure 21. Shift Frame Clock One Bit Left.

See Figures 20 and 21.

This control is only available for the **Frame Clock**. The leading edge of the Frame clock is normally aligned with the leading edge of the first data bit (or first padding bit, if the data is preceded in the frame by padding) of the first channel, channel 0.

If **Shift One Bit Left** is checked, the time relationship between the Frame Clock and the data is changed so that the leading edge of the Frame Clock is aligned one bit before the first data bit of channel 0. A typical timing diagram would show the Frame Clock pulse as shifted one bit to the left.

The I^2S bus standard specifies that the Frame Clock is shifted one bit to the left.

Bit Wide Pulse (Frame Clock and Channel Clock)

See Figures 20 and 23.

This control is available for the Frame Clock and the Channel Clock, when either of these clocks is an OUTPUT. It establishes whether the clock pulse has an approximately 50% duty cycle, or if the leading pulse for the clock has a width of one data bit (one period of the bit clock).

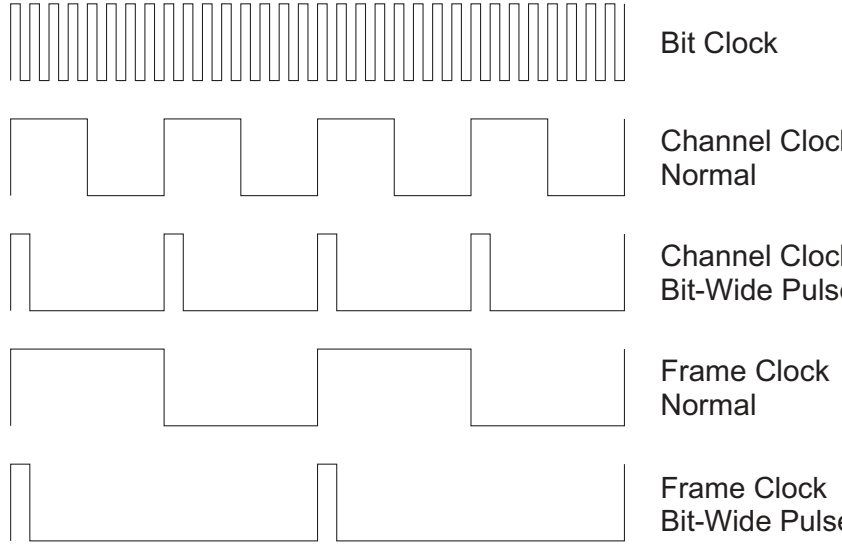


Figure 23. Channel Clock and Frame Clock Normal Pulse width and Bit-Wide Pulse.

PSIA Clock Rate and Factor Settings

See Figure 20.

PSIA can transmit and receive a number of clock rates. Depending upon configuration, these rates can be set or influenced by user entry, instrument

hardware state, selections for number of channels per frame and number of bits per channel, and DUT settings.

Each clock setting is discussed below.

Frame Clock (Fs) Rate Setting

See Figure 20.

You must specify a frame clock rate (Fs) for the Transmitter or Receiver when you configure the PSIA for a test.

PSIA Transmitter or Receiver as a Master: All Clocks set to OUT

When all clocks of the PSIA Transmitter or Receiver sections are set to OUT, that PSIA section is acting as a master, with the DUT as slave. In this case, entering an Fs value sets the actual PSIA frame clock rate for the Transmitter or Receiver. This rate ripples to the Channel Clock, Bit Clock, N*Fs and Master Clock outputs, multiplied by the factors entered in the Channels, Bits and "N" fields.

Valid Fs values range from 6.75 kHz to 216 kHz. Even given a valid Fs, it is still possible to specify values for **channels** and **bits / channel** that cause the instrument master clock to exceed its maximum frequency. In such a case the PSIA Master Clock **Computed Rate** display will show an invalid clock frequency, indicated by a dashed line "--------Hz".

See **Maximum Clock Frequency** on page 48.

PSIA Transmitter or Receiver as a Slave: One or more clocks set to IN

When any clock in the Transmitter or Receiver section is set to IN, that PSIA section is acting as a slave, with the DUT (or another external clock) as master. In these cases, entering a Frame Rate value sets a nominal reference for calculation of the PSIA clock rate displays. The actual Fs is obtained by dividing the external clock rate by the factors entered in the "**M**" or Master Clock Mulitplier field, the **bits / channel** and **channels** fields.

If your configuration does not require a Master Clock connection between the PSIA and the DUT, set the master clock direction the same as the Bit Clock direction.

Channels per Frame

See Figure 20.

You must specify the number of **channels** per frame for each PSIA converter test. The valid entry range for the **channels** field in the PSIA is **1** to **256.**

The number of channels per frame is a factor in determining the Bit Clock rate and the Master Clock rate. In a particular configuration, setting the number of channels per frame too high may cause either or both of these clocks to exceed the Maximum Clock Frequency. In such a case the PSIA clock Computed Rate display will show an invalid clock frequency, indicated by a dashed line "--------Hz".

Setting the Bits per Channel

See Figure 20.

You must specify the number of bits per channel for each PSIA converter test. This value is the length of the entire channel data word in bits. It is the sum of the number of audio data bits (the data length) and padding bits, if any.

The valid entry range for the **bits / channel** field in the PSIA is **8** to **32**; however, the number of bits per channel must always be greater than or equal to the data length. If it is less than the data length, the number of bits per channel is set to the same value as the data length. If the number of bits per channel is greater than the data length but less than the sum of the data length and the padding, the padding is reduced, with trailing bits removed before leading bits.

Also, the number of bits per channel is a factor in determining the Bit Clock rate and the Master Clock rate. In a particular configuration, setting the number of bits per channel too high may cause either or both of these clocks to exceed the Maximum Clock Frequency. In such a case the PSIA clock Computed Rate display will show an invalid clock frequency, indicated by a dashed line "--------Hz".

N, the N*Fs multiplier

N*Fs is a reference clock signal output available from both the PSIA Transmitter and Receiver that can be used for synchronization of external devices. Set to the appropriate frequency, N*Fs can be used as a master clock signal for a DUT.

N*Fs is a multiple of the Frame Rate (Fs), by N, the user-supplied multiplier. Enter N in the N*Fs Setting field.

*PSIA generates the N*Fs clock from either the instrument system clock or the PSIA Master Clock INPUT by using a programmable divider that can be set only to integers from 1 to 256. If you specify a value for N that cannot be achieved with an integer divider in this range, the PSIA will show an invalid clock frequency for N*Fs, indicated by a dashed line "--------Hz".*

N*Fs is always an OUTPUT. When the Master Clock is an OUTPUT, it runs at the same rate as N*Fs.

M, the Master Clock multiplier

The Master Clock multiplier, or M, is a factor used in calculating the relationship between Fs and the Master Clock, when the Master Clock is set to IN.

For example, consider a test in which you are slaving the PSIA to a converter that is providing a Master Clock at 5.6448 MHz, and you want to have Fs be 44.1 kHz . Enter **128** into the Master Clock multiplier setting field to establish this relationship. Clock rates will be divided from the external Master Clock using calculations based on the computed Fs.

This setting field is “grayed out” and unavailable when Master Clock is an OUTPUT. Under this condition the Master Clock runs at the same rate as N*Fs.

Jittering the Master Clock

Any jitter impairment selected in the DIO **Jitter Generation** field will jitter the master clock output and all clocks derived from the master clock.

Set the DIO **Jitter Generation** control to **OFF** for normal operation.

*Although the **Jitter Clock Outputs** checkbox on the Sync/ Ref panel is not available when the PSIA transmitter is enabled, jitter is still applied to the master clock if the DIO jitter generator is **ON**. To be sure that there is no jitter impairment added to the master clock output, set the DIO **Jitter Generation** control to **OFF**.*

Computed Clock Rate Displays

All clock signals available at PSIA clock OUT ports are either divisions of the instrument Master Clock, or divisions of externally-provided clock signals. The panel displays associated with clock outputs are computed values, calculated by multiplying the user-entered nominal **Frame Clock rate (Fs)** by the **bits / channel** and **channels** factors.

Similarly, all the PSIA clock IN ports are set to receive clock rates that are divisions of an internal or external master clock, and the panel displays show calculated values representing the nominal frequency of each clock, based on the user-entered **Fs** and **bits / channel** and **channels** factors.

These displays are accurate if the master clock (or bit clock, if PSIA is slaved to a bit clock) frequency is accurate and the user settings are correct.

Certain combinations of user settings will push computed clock rates beyond the specified maximum rate for the associated hardware. When this occurs the PSIA clock Computed Rate display will show an invalid clock frequency, indicated by a dashed line "--------Hz".

See Maximum Clock Frequency on page 48.

Logic Voltage controls

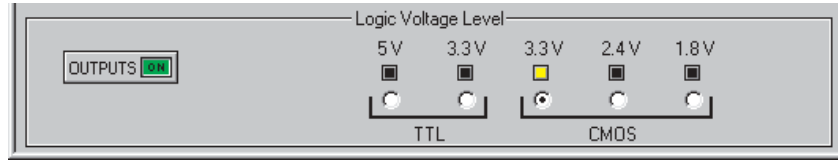


Figure 24. The PSIA Logic Voltage controls.

The PSIA-2722 can accommodate TTL logic at 5 V and 3.3 V voltage levels, and CMOS logic at 3.3 V, 2.4 V and 1.8 V voltage levels.

For circuit protection, tests are loaded with the output voltages OFF. When output voltages are ON, a user selection of a higher voltage resets the output voltages to OFF.

PSIA Quick Setup Guide

The Quick Setup Guide is a series of steps to help you get typical converter test setups ready quickly. These steps and other aspects of operating PSIA-2722 are covered in more detail in previous topics in this chapter.

1

Set up the instrument and PSIA

The instrument must be properly connected to a PC that has AP2700 or APWIN 2.22 or later installed. Connect the four cables between the instrument and the PSIA. Apply mains power to both units. See **Connecting the PSIA to the Instrument** on page 7. Start the control software and open a New Test.

2

Connect an oscilloscope

It is useful to view the clock and data waveforms simultaneously on a multichannel oscilloscope while configuring and testing the PSIA. See **Oscilloscope Monitoring** on page 46.

3

Open both the PSIA Transmitter and Receiver panels for a Loop-Back Test to verify initial configuration

Begin with a loop-back test, which requires the use of both the PSIA Transmitter and Receiver sections. On the DIO panel, choose PSIA in both the **In-**

put: Connector (APWIN: **Input: Format**) list and the **Output: Connector** (APWIN: **Output: Format**) lists. This will enable both Transmitter and Receiver panels.

Connect three loop-back cables between the PSIA Transmitter and Receiver Bit Clock, Frame Clock and Data ports. See the illustration in PSIA Loop-Back on page 11.

> *In a **New Test**, the PSIA Transmitter and Receiver sections have compatible settings by default, ready for a loop-back test.*

Run a simple test (such as transmitting and receiving a 1 kHz sine wave) through the PSIA loop-back. This will verify that the PSIA is properly connected and that your test is compatible and properly configured.

Use Loop-Back mode to verify your custom configuration

4

With the loop-back cables still connected, re-set the PSIA controls for the data configuration, clock rates and logic voltages required for your test of the DUT. Run your test again to verify that the test is still compatible and properly configured for these new settings.

Connect your device

5

Set any jumpers or switches necessary for the test on your DUT. Connect your DUT to the proper PSIA ports and make any other direct audio or digital connection from the DUT to the instrument that are necessary for your test. See **Oscilloscope Monitoring**, **Connections for DAC Testing**, or **Connections for SRC Testing**.

- For SRC or loop-back testing, both the PSIA Transmitter and Receiver panels are necessary. You will need to keep **PSIA** as the selection in both the DIO **Input: Connector** and **Output: Connector** (APWIN: **Input: Format** and **Output: Format**) lists.
- For ADC testing, only the PSIA Receiver panel is necessary. You may close the Transmitter panel.

For DAC testing, only the PSIA Transmitter panel is necessary. You may close the Receiver panel.

Apply power to the DUT and begin your testing

6

Common converter testing configurations

These are common configurations for many converter tests. See page 39 for definitions of the PSIA abbreviations and terms used here.

PSIA Transmitter: Frame, Bit & Master Clock OUT

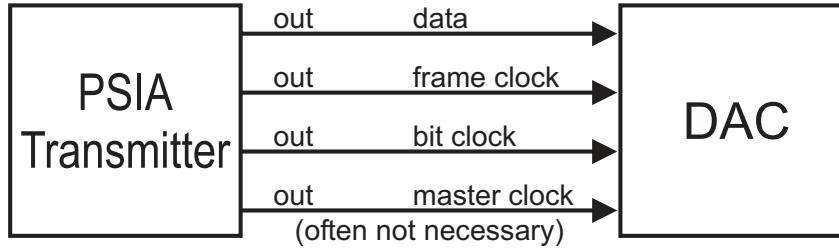


Figure 25. Transmitter: Frame, Bit and Master Clock OUT.

In this configuration the PSIA is the master, outputting all clocks, which are derived from the instrument system clock. In many cases, the master clock connection is not used, with the DUT slaved instead to the PSIA bit clock.

- Frame clock rate (Fs) is set in the **Frame Clock Rate** field.
- Bit clock rate = Fs × channels × bits.
- Master clock rate =Fs × N

PSIA Transmitter: Frame & Bit Clock OUT, Master Clk IN

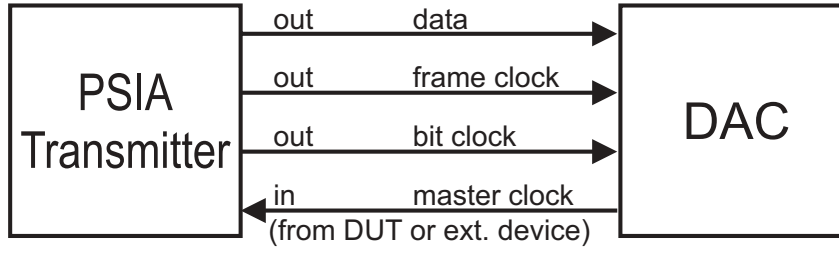


Figure 26. Transmitter: Frame and Bit Clock OUT, Master Clock IN.

In this configuration the PSIA is the slave, with either the DUT or an external device providing the master clock, from which the other clocks are derived and output by the PSIA.

- Frame clock rate (Fs) field is a nominal entry for calculation purposes. Nominal Fs should be master clock ÷ M.

- Master clock multiplier field (M) is available for numerical entry.
- Actual Fs = master clock ÷ M.
- Bit clock rate = Fs × channels × bits.
- Master clock rate is determined by external settings.

PSIA Receiver: Frame, Bit & Master Clock OUT

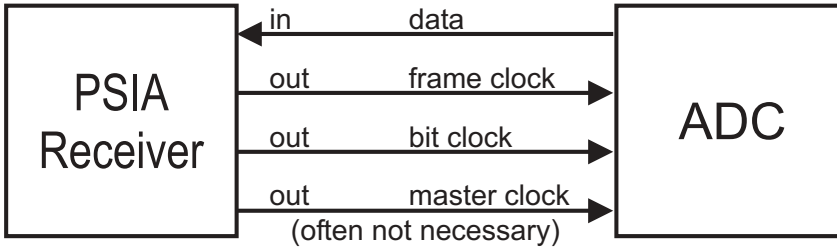


Figure 27. Receiver: Frame, Bit and Master Clock OUT.

In this configuration the PSIA is the master, outputting all clocks, which are derived from the instrument system clock. In many cases, the master clock connection is not used, with the DUT slaved instead to the PSIA bit clock.

- Frame clock rate (Fs) is set in the **Frame Clock Rate** field.
- Bit clock rate = Fs × channels × bits.
- Master clock rate = Fs × N.

PSIA Receiver: Frame & Bit Clock OUT, Master Clock IN

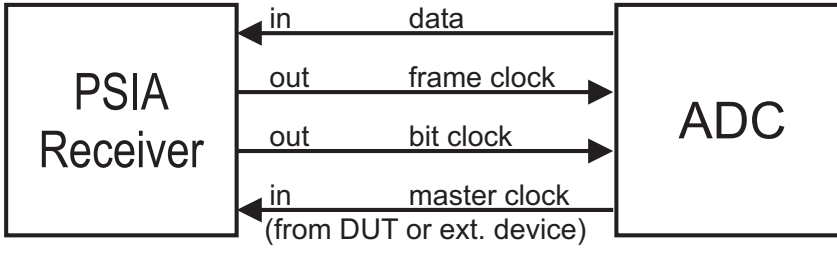


Figure 28. Receiver: Frame and Bit Clock OUT, Master Clock IN.

In this configuration the PSIA is the slave, with either the DUT or an external device providing the master clock, from which the other clocks are derived and output by the PSIA.

- Frame clock rate (Fs) field is a nominal entry for calculation purposes. Nominal Fs should be master clock ÷ M.
- Master clock multiplier field (M) is available for numerical entry.
- Actual Fs = master clock ÷ M.
- Bit clock rate = Fs × channels × bits.
- Master clock rate is determined by external settings.

Appendix A

Miscellany

PSIA Abbreviations and Terms

- Fs = Frame Clock or Frame Clock Rate or Sample Rate.
- bclk = Bit Clock or Bit Clock Rate.
- mclk = Master Clock or Master Clock Rate.
- M = Master Clock Multiplier.
- N = N*Fs Multiplier.
- channels = number of channels (as entered in factor field).
- bits = number of bits (as entered in factor field).
- DUT = device under test: an ADC, DAC, etc.
- ADC = analog to digital converter.
- DAC = digital to analog converter.
- SRC = sample rate converter.

Oscilloscope Examples

These examples show PSIA clock and data outputs in various configurations. The oscilloscope used is a Tektronix TDS 2024 Four Channel Digital Storage Oscilloscope, triggered on the Frame Clock.

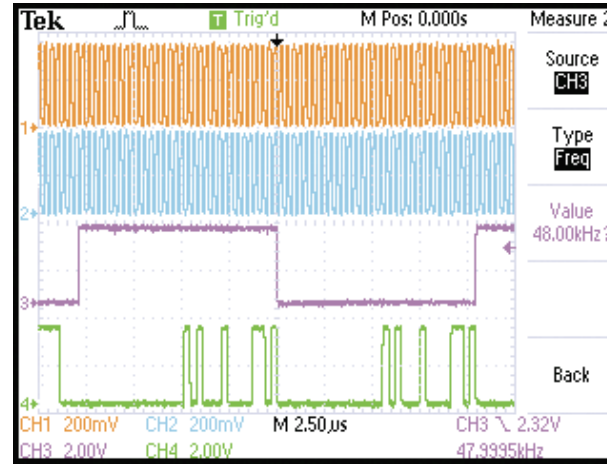


Figure 29. Master clock, bit clock, frame clock, 48 kHz Fs, 32-bit word, 16-bit data, right justified.

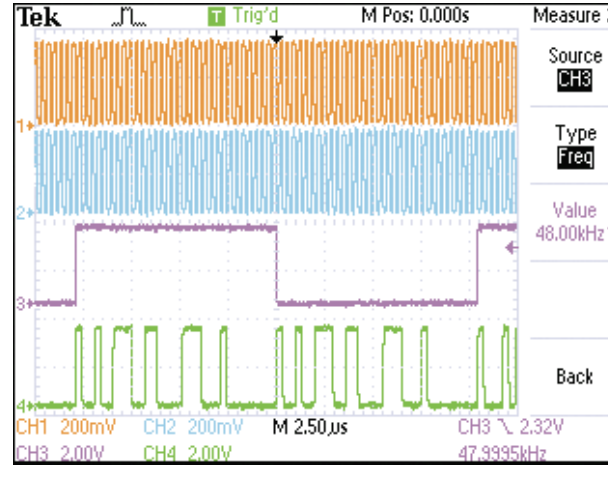


Figure 30. Master clock, bit clock, frame clock, 48 kHz Fs, 32-bit word, 24-bit data, left justified.

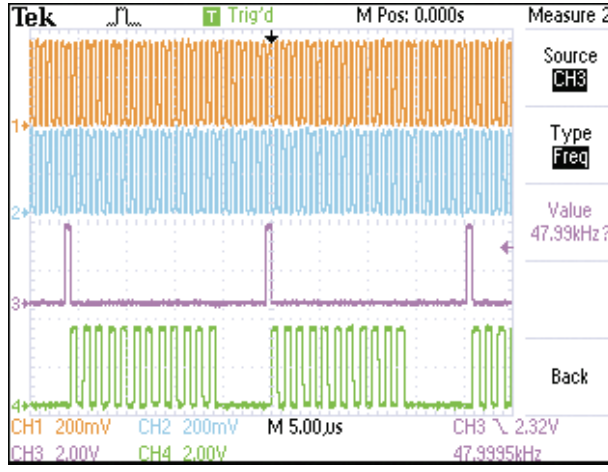


Figure 31. Master clock, bit clock, frame clock, 48 kHz Fs, 32-bit word, 24-bit data, left justified, bit-wide frame clock pulse.

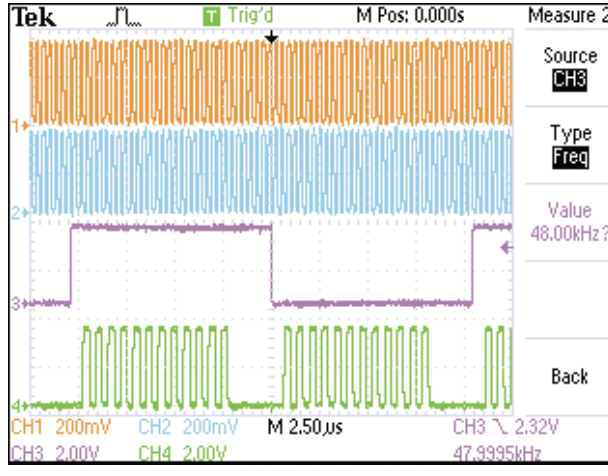


Figure 32. Master clock, bit clock, frame clock, 48 kHz Fs, 32-bit word, 24-bit data, left justified, I²S (shift one bit left).

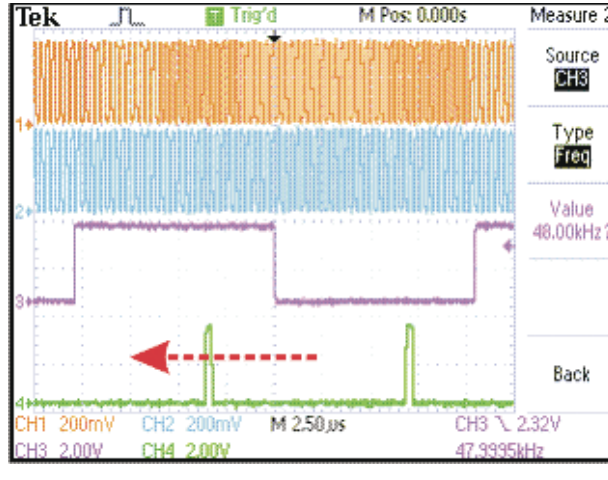


Figure 33. Master clock, bit clock, frame clock, 48 kHz Fs, 32-bit word, 24-bit data, walking-one data moving right-to-left (MSB first) (red arrow added).

N*Fs Table

The table below shows the master clock frequencies (N*Fs) for a variety of combinations of sample rates (Fs) and multipliers (N). Shaded cells indicate frequencies that are compatible with PSIA-2722 operation but must be provided by an external clock.

	N*Fs (master clock frequency; mclk) in MHz, where:					
	N=128	N=192	N=256	N=384	N=512	N=768
Fs=32 kHz	4.096	6.144	8.192	12.288	16.384	24.576
Fs=44.1 kHz	5.6448	8.467	11.2896	16.9340	22.5792	33.8688
Fs=48 kHz	6.114	9.216	12.288	18.432	24.576	36.8640
Fs=96 kHz	12.288	18.432	24.576	36.864	49.1520	unavailable
Fs=192 kHz	24.576	36.864	49.1520	unavailable	unavailable	unavailable

Using INTERVU with PSIA-2722

The instrument Intervu ADC is connected to the AES3 / IEC60958 digital inputs, and will not read **PSIA** data when the DIO **Input: Connector** (APWIN: **Input: Format**) is set to PSIA. If you want to look at a PSIA serial waveform using Intervu, connect the serial line directly to the Digital Input BNC on the front of the instrument. Select **BNC (unbal)** as the DIO instrument. You can now use Intervu to analyze the serial waveform.

Note: the Intervu ADC and analysis program are optimized for AES3 / IEC60958 digital waveforms and have a maximum bandwidth of 30 MHz. This limits useful waveform views to serial waveforms with a maximum bit rate of under about 8 MHz. Jitter can be analyzed at somewhat higher rates.

Appendix B

Configuration Examples and Files

Eval boards and sample files

The Audio Precision technical support staff have evaluated a number of converters using the PSIA, and their recommendations for PSIA configuration are available on the Audio Precision Web site at audioprecision.com. Browse to Products: Measurement Instruments: PSIA-2722: Device Connectivity.

The recommendations include illustrations with jumper and DIP-switch settings and links to manufacturers' documents. A sample test file with PSIA parameters configured to the device is also linked to each page.

There are currently configurations on the Web site for ADCs, DACs and SRCs from manufacturers such as AKM, Analog Devices, Burr-Brown, Crystal, Philips, Texas Instruments and others. An example Web page for the AKM AK4393 DAC is shown on the next page.

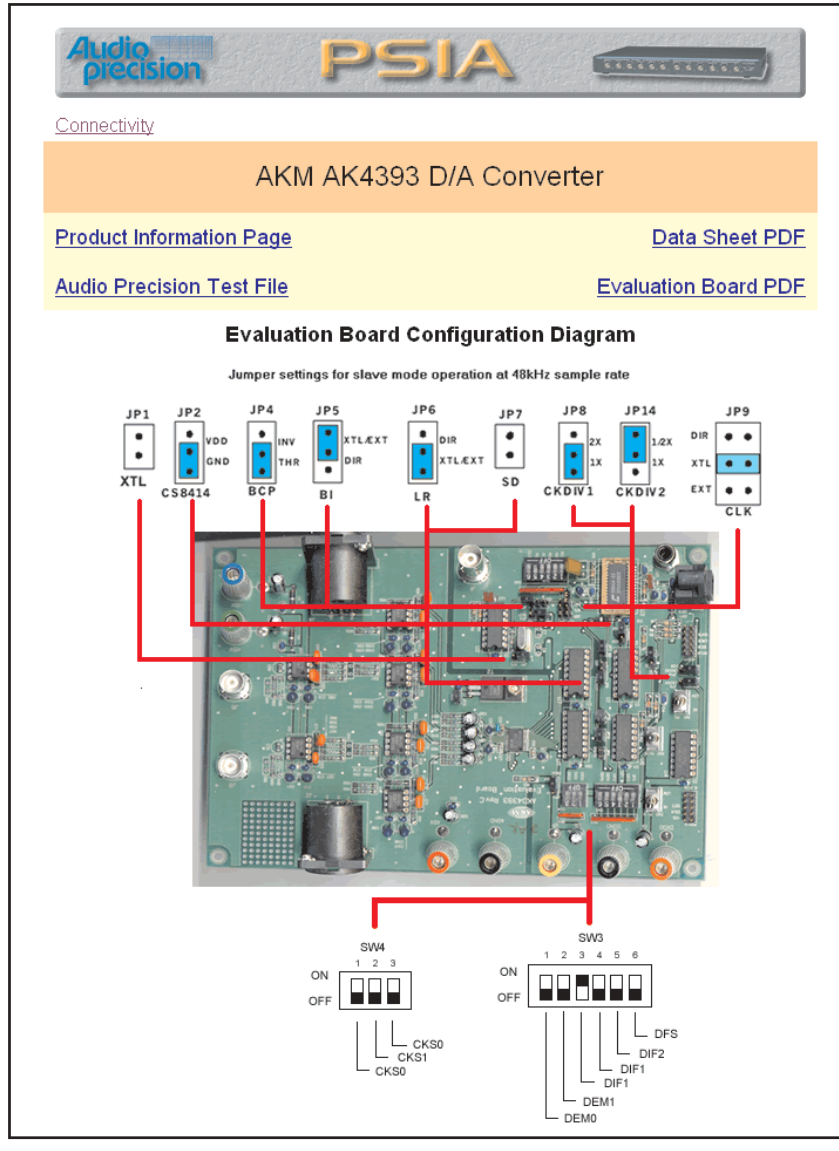


Figure 34. Typical converter evaluation board Web page, this one being for the AK4393. Links lead to manufacturer documentation.

Appendix C

Connection Guidelines

General Guidelines

Proper transmission of high-frequency clock and data signals requires careful attention to line and termination impedance. Connectors and cables must meet rigorous specifications, and good transmission line practice must be observed in making connections.

Here are some guidelines:

- Use high-quality cable and connector components.
- Use 50 Ω coaxial cable (RG-58), such as Belden 8259 or 9311.
- Use the same length of cable for all clock and data lines to match propagation delay.
- Never “Y” or “T” clock or data connections.
- For signal monitoring, connect the oscilloscope with compatible probes to the PSIA probe pick-off jacks, as described below.

Oscilloscope Monitoring

It is useful to view the clock and data waveforms simultaneously on a multichannel oscilloscope while configuring and testing the PSIA.

- A four-channel scope is optimal, displaying Bit Clock, Channel Clock, Frame Clock and Data.
- Alternatively, a two-channel scope is sufficient, displaying Frame Clock and Data.

Triggering

Trigger from the Frame Clock channel.

Oscilloscope Connections

The PSIA-2722 provides oscilloscope probe pick-off jacks for monitoring the clock and data ports. A 2.5 mm probe jack is located adjacent to the BNC connector for each port. These jacks are intended to interface directly with any probe and scope combination that provides

- a minimum of 100 MHz system bandwidth,
- a minimum of 100 kΩ resistive loading, and
- less than 14 pF capacitive loading at the probe tip.

Be sure your 2.5 mm probe and oscilloscope are compatible with each other and meet these bandwidth and loading guidelines. Improper loading can adversely affect the clock or data waveform being monitored, producing inaccurate oscilloscope traces and possible adverse effects in the behavior of the DUT or the analyzer.

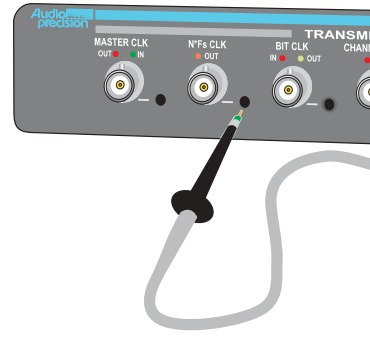


Figure 35. Inserting a 2.5 mm probe tip into a PSIA probe pick-off jack. Note that some probes will require partial disassembly (removal of spring hook or grounding pigtail) to be compatible with the probe pick-off jacks.

As an example, the Tektronix TDS2024/P6133 scope/probe combination satisfies these requirements, providing a system bandwidth of 120 MHz and 12.7 pF probe loading.

Appendix D

Specifications

DC Characterisics

DC characteristics, no load

Parameter	1.8 V CMOS		2.4 V CMOS		3.3 V CMOS		3.3 V TTL		5 V TTL	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
HIGH Level Input	0.9	—	1.2	—	1.6	—	1.6	—	1.8	—
LOW Level Input	—	0.9	—	1.2	—	1.6	—	1.6	—	1.8
HIGH Level Output	1.6	1.9	2.2	2.6	3.0	3.5	3.0	3.5	3.4	3.9
LOW Level Output	0.0	0.2	0.0	0.2	0.0	0.2	0.0	0.2	0.0	0.2
Absolute Maximum	–0.4	5.5	–0.4	5.5	–0.4	5.5	–0.4	5.5	–0.4	5.5

Table 1. PSIA DC characteristics, no load.

PSIA input / output impedance

Signal	Input Impedance (Ω)	Output Impedance (Ω)	Max V In
Tx Master Clock	>10 k	50	5.5 V
Tx NFs Clock	N/A	50	N/A
Tx Bit Clock	>10 k	50	5.5 V
Tx Channel Clock	N/A	50	N/A
Tx Frame Clock	30 k	50	5.5 V
Tx Data	N/A	50	N/A
Rx Master Clock	30 k	50	5.5 V

Signal	Input Impedance (Ω)	Output Impedance (Ω)	Max V In
Rx NFs Clock	N/A	50	N/A
Rx Bit Clock	>10 k	50	5.5 V
Rx Channel Clock	N/A	50	N/A
Rx Frame Clock	30 k	50	5.5 V
Rx Data	30 k	N/A	5.5 V

Table 2. PSIA input / output impedance (continued from previous page).

AC characteristics

Maximum clock frequency

Master Clock In (external clock)	60 MHz
Master Clock Out	27.648 MHz (instrument limit)
Bit Clock In/Out	25 MHz (using external master clock)
	13.824 MHz (using instrument master clock)
Frame Clock In/Out	216 kHz

Table 3. Maximum clock frequency

Output latency, Clock to Out

Signal	From	Typical
N*Fs	Master Clock IN	20 ns
	Master Clock OUT	0 ns
Bit Clock	Master Clock IN	20 ns
	Master Clock OUT	Note 1
Channel Clock	Bit Clock IN	15 ns
	Bit Clock OUT	15 ns
Frame Clock	Bit Clock IN	15 ns
	Bit Clock OUT	15 ns
Data	Bit Clock IN	15 ns
	Bit Clock OUT	15 ns
Note 1: The Bit Clock is synchronous with the Master Clock Out, but does not have a guaranteed phase relationship.		

Table 4. Output latency, Clock to Out

Setup and Hold, inputs

Signal	Parameter	Before	Max
Frame Clock, Data	Setup	Bit Clock	3 ns
	Hold	Bit Clock	7 ns

Table 5. Setup and Hold, Inputs

User test jacks

The scope probe pick-off jacks are intended to interface with any 2.5 mm probe and scope combination which provide a minimum of 100 MHz bandwidth, at least 100 kΩ resistive loading and less than 14 pF capacitance loading at the probe tip.

APIB

APIB configuration maximums

Maximum APIB bus configuration with PSIA:

- 1 instrument (2700 Series or System Two Cascade *Plus*)
- 1 PSIA-2722
- 16 Audio Precision switchers
- 1 DCX-127
- a total of 33' (10 m) of APIB cable (not including the 1' [.3 m] patches.

Appendix E

AP Basic Extensions for PSIA

This chapter describes OLE commands which have been added to AP Basic Extensions to provide programmatic control for PSIA features.

AP.PSIA.MasterClkDir — Property

Syntax `AP.PSIA.MasterClkDir`

Data Type

Integer	Transmit-side master clock	Receive-side master clock
0	Input	Input
1	Output	Input
2	Input	Output

Description This command selects the master clock direction for transmit and receive sides simultaneously. Each master clock port can be configured as an input or as an output, although not all combinations are available. See the table above. In input (slave) mode, the master clock is provided by an external source. In output (master) mode, the master clock is provided by the PSIA.

See Also

`AP.PSIA.Rx.MasterClk.Factor, AP.PSIA.Rx.BitClkDir, AP.PSIA.Rx.FrameClkDir`

Example

```
Sub Main
  AP.S2CDio.OutFormat = 3    ' PSIA output
  AP.PSIA.MasterClkDir = 1   ' Tx out, Rx in
  AP.PSIA.OutputsOn = True   ' Outputs on
```

```
    AP.PSIA.VoltageSetting = PSIA_3_3_TTL
                             ' 3.3 V TTL
    AP.PSIA.Tx.MasterClk.Factor = 256
                             ' master clk = 256 * Fs
    AP.PSIA.Tx.NFsClk.Factor = 128
                             ' N*Fs clk = 128 * Fs
    AP.PSIA.Tx.NFsClk.InvWfm = False
                             ' non-inverted
    AP.PSIA.Rx.MasterClk.Factor = 128
                             ' N*Fs clk = 128 * Fs
    AP.PSIA.Rx.NFsClk.Factor = 128
                             ' master clk = 128 * Fs
    AP.PSIA.Rx.NFsClk.InvWfm = True
                             ' inverted
End Sub
```

AP.PSIA.OutputsOn

Property

Syntax **AP.PSIA.OutputsOn**

Data Type Boolean

True	On
False	Off

Description This command turns the PSIA outputs on or off. When the outputs are off, they are tri-stated. When the outputs are on, they are driven according to the voltage setting.

See Also AP.PSIA.VoltageSetting

Example See AP.PSIA.MasterClkDir.

AP.PSIA.Rx.BitClk.Dir
AP.PSIA.Tx.BitClk.Dir

Property

Syntax **AP.PSIA.Rx.BitClk.Dir**

AP.PSIA.Tx.BitClk.Dir

Data Type Integer

0	Output
1	Input

Description This command selects the bit clock direction. Each bit clock port can be configured as an output or as an input. In output (master) mode, the bit clock is provided by the PSIA. In input (slave) mode, the bit clock is provided by an external source.

See Also `AP.PSIA.Rx.BitClk.Factor, AP.PSIA.Rx.FrameClk.Dir, AP.PSIA.Rx.MasterClkDir`

Example

```
Sub Main
  AP.PSIA.Tx.BitClk.Dir = 0      ' output
  AP.PSIA.Tx.BitClk.Factor = 32  ' 32-bit words
  AP.PSIA.Rx.BitClk.Dir = 1      ' input
  AP.PSIA.Rx.BitClk.Factor = 32  ' 32-bit words
End Sub
```

AP.PSIA.Rx.BitClk.Factor
AP.PSIA.Tx.BitClk.Factor

Property

Syntax **`AP.PSIA.Rx.BitClk.Factor`**
`AP.PSIA.Tx.BitClk.Factor`

Data Type Integer 8-32 (limited also by digital resolution settings)

Description This command specifies the ratio (factor) between the bit clock and the channel clock. It is equal to the number of bits per channel. It cannot be set lower than the number of bits specified in the digital output resolution field (for Tx) or the digital input resolution field (for Rx). The maximum number of bits per channel is 32.

See Also `AP.PSIA.Rx.BitClk.Dir, AP.S2CDio.InResolution, AP.S2CDio.OutResolution`

Example See AP.PSIA.Rx.BitClk.Dir.

AP.PSIA.Rx.ChannelClk.BitWidePulse
AP.PSIA.Tx.ChannelClk.BitWidePulse

Property

Syntax

AP.PSIA.Rx.ChannelClk.BitWidePulse

AP.PSIA.Tx.ChannelClk.BitWidePulse

Data Type

Boolean

True	Bit Wide Pulse (one period of the bit clock)
False	Approximately 50% duty cycle

Description

This command selects the pulse width of the channel clock output. Assuming that the channel clock output is not inverted, the following are true:

- When ChannelClk.BitWidePulse is *True*, the channel clock is high for the first bit of each subframe, and low for the rest of the subframe.
- When ChannelClk.BitWidePulse is *False*, and the number of bits B is even, the channel clock is high for the first B/2 bits, and low for the rest of the subframe.
- When Channel.BitWidePulse is *False*, and the number of bits B is odd, the channel clock is high for the first (B-1)/2 bits, and low for the rest of the subframe.

See Also

AP.PSIA.Rx.ChannelClk.EdgeSync,
AP.PSIA.Rx.ChannelClk.Factor,
AP.PSIA.Rx.ChannelClk.InvWfm

Example

```
Sub Main
  AP.PSIA.Tx.ChannelClk.BitWidePulse = False
                        ' 50% duty cycle
  AP.PSIA.Tx.ChannelClk.EdgeSync = 0
                        ' assert on rising edge
  AP.PSIA.Tx.ChannelClk.Factor = 2
                        ' 2 channels
  AP.PSIA.Tx.ChannelClk.InvWfm = True
                        ' invert channelclk
  AP.PSIA.Tx.ChannelClk.BitWidePulse = False
                        ' 50% duty cycle
  AP.PSIA.Rx.ChannelClk.EdgeSync = 1
                        ' latch on falling edge
```

```
    AP.PSIA.Rx.ChannelClk.Factor = 2
                          ' 2 channels
    AP.PSIA.Rx.ChannelClk.InvWfm = False
                          ' inverted channelclk
End Sub
```

AP.PSIA.Rx.ChannelClk.EdgeSync
AP.PSIA.Tx.ChannelClk.EdgeSync

Property

Syntax **AP.PSIA.Rx.ChannelClk.EdgeSync**
AP.PSIA.Tx.ChannelClk.EdgeSync

Data Type Integer

0	Rising edge
1	Falling edge

Description For the transmitter side (Tx), this command selects whether the channel clock output is asserted at the rising or falling edge of the bit clock. For the receiver side (Rx), this command selects whether the channel clock input is latched at the rising or falling edge of the bit clock.

See Also `AP.PSIA.Rx.ChannelClk.BitWidePulse`, `AP.PSIA.Rx.ChannelClk.Dir`, `AP.PSIA.Rx.ChannelClk.InvWfm`.

Example See AP.PSIA.Rx.ChannelClk.BitWidePulse.

AP.PSIA.Rx.ChannelClk.Factor
AP.PSIA.Tx.ChannelClk.Factor

Property

Syntax **AP.PSIA.Rx.ChannelClk.Factor**
AP.PSIA.Tx.ChannelClk.Factor

Data Type Long 1–256

Description This command specifies the ratio (factor) between the channel clock and the frame clock. It is equal to the number of channels per frame. The minimum number of channels is 1. The maximum number of channels is 256; limitations on the master clock rate may further restrict this.

See Also `AP.PSIA.Rx.ChannelClk.BitWidePulse`, `AP.PSIA.Rx.ChannelClk.EdgeSync`, `AP.PSIA.Rx.ChannelClk.InvWfm`.

Example See AP.PSIA.Rx.ChannelClk.BitWidePulse, AP.PSIA.Rx.ChannelClk.InvWfm.

AP.PSIA.Rx.ChannelClk.InvWfm
AP.PSIA.Tx.ChannelClk.InvWfm

Property

Syntax **AP.PSIA.Rx.ChannelClk.InvWfm**
AP.PSIA.Tx.ChannelClk.InvWfm

Data Type Boolean

True	Inverted channel clock
False	Non-inverted channel clock

Description This command sets the polarity of the channel clock. When set to *False* (non-inverted), the channel clock is high at the start of the subframe, and low for the rest of the subframe. When set to *True* (inverted), the channel clock is low at the start of the subframe, and high for the rest of the subframe.

See Also `AP.PSIA.Rx.ChannelClk.BitWidePulse`, `AP.PSIA.Rx.ChannelClk.EdgeSync`, `AP.PSIA.Rx.ChannelClk.Factor`

Example See AP.PSIA.Rx.ChannelClk.BitWidePulse.

AP.PSIA.Rx.Data.ChannelA
AP.PSIA.Tx.Data.ChannelA

Property

Syntax **`AP.PSIA.Rx.Data.ChannelA`**
`AP.PSIA.Tx.Data.ChannelA`

Data Type Integer — 0 to n–1, where n is one less than the number of channels specified by the associated ChannelClk.Factor command

Description For the transmitter side (Tx), this command causes generator Channel A data to appear on the selected subframe. For the receiver side (Rx), this command causes data from the selected subframe to be applied to Channel A of the analyzer.

Note that the channel assignments are zero-based, that is, the channels are numbered from zero to one less than the number of available channels.

See Also `AP.PSIA.Rx.Data.ChannelB`

Example See AP.PSIA.Rx.Data.EdgeSync.

AP.PSIA.Rx.Data.ChannelB
AP.PSIA.Tx.Data.ChannelB

Property

Syntax **`AP.PSIA.Rx.Data.ChannelB`**
`AP.PSIA.Tx.Data.ChannelB`

Data Type Integer — A+1 to n–1, where A is the number of channels specified for Channel A and n is one less than the number of channels specified by the associated ChannelClk.Factor command

Description For the transmitter side (Tx), this command causes generator Channel B data to appear on the selected subframe. For the receiver side (Rx), this command causes data from the selected subframe to be applied to Channel B of the analyzer.

Note that the channel assignments are zero-based, that is, the channels are numbered from zero to one less than the number of available channels.

See Also `AP.PSIA.Rx.Data.ChannelA`

Example See AP.PSIA.Rx.Data.EdgeSync.

AP.PSIA.Rx.Data.EdgeSync
AP.PSIA.Tx.Data.EdgeSync

Property

Syntax **`AP.PSIA.Rx.Data.EdgeSync`**
`AP.PSIA.Tx.Data.EdgeSync`

Data Type Integer

0	Rising edge
1	Falling edge

Description For the transmitter side (Tx), this command selects whether the data output is asserted at the rising or falling edge of the bit clock. For the receiver side (Rx), this command selects whether the data input is latched at the rising or falling edge of the bit clock.

See Also `AP.PSIA.Rx.ChannelClk.EdgeSync`, `AP.PSIA.Rx.FrameClk.EdgeSync`

Example

```
Sub Main
  AP.PSIA.Tx.ChannelClk.Factor = 4
              ' 4 channels...
  AP.PSIA.Tx.BitClk.Factor = 32
              ' ...of 32-bit data
  AP.PSIA.Tx.Data.EdgeSync = 0
              ' assert on rising edge
  AP.PSIA.Tx.Data.ChannelA = 1
              ' assign ChA data to channel 1
```

```
  AP.PSIA.Tx.Data.ChannelB = 3
              ' assign ChB data to channel 3
  AP.PSIA.Tx.Data.MsbFirst = True
                ' send audio word MSB first
  AP.PSIA.Tx.Data.PrePadType = 2
                ' pre-pad with sign
  AP.PSIA.Tx.Data.PostPadType = 0
                ' post-pad with zeros
     ' Note: the following two lines are equivalent
  AP.PSIA.Tx.Data.Justify(apbRight)
                ' right justify audio word
  AP.PSIA.Tx.Data.PadBits =
  AP.PSIA.Tx.BitClk.Factor -
  AP.S2CDio.OutResolution
  AP.PSIA.Rx.ChannelClk.Factor = 4
                ' 4 channels...
  AP.PSIA.Rx.BitClk.Factor = 32
                ' ...of 32-bit data
  AP.PSIA.Rx.Data.EdgeSync = 1
                ' latch on falling edge
  AP.PSIA.Rx.Data.ChannelA = 1
                ' channel 1 data -> ChA of analyzer
  AP.PSIA.Rx.Data.ChannelB = 3
                ' channel 1 data -> ChB of analyzer
  AP.PSIA.Rx.Data.MsbFirst = True
              ' accept audio word MSB first
              ' Note: the following two lines are
equivalent
  AP.PSIA.Rx.Data.Justify(apbRight)
              ' accept right-justified audio word
  AP.PSIA.Rx.Data.PadBits =
  AP.PSIA.Rx.BitClk.Factor -
  AP.S2CDio.InResolution
End Sub
```

AP.PSIA.Rx.Data.Justify
AP.PSIA.Tx.Data.Justify

Method

Syntax

AP.PSIA.Rx.Data.Justify(ByVal *Justify* As Constant**)**

AP.PSIA.Tx.Data.Justify(ByVal *Justify* As Constant**)**

Parameter

Name	Description
Justify	apbLeft: Left justify audio word apbRight: Right justify audio word

Description

This command justifies the audio data to the first bit of the subframe (apbLeft) or the last bit of the subframe (apbRight). For left justification, any padding bits trail the audio word. For right justification, any padding bits lead the audio word. Note that justification does not affect the bit order in the word (that is, whether the MSB or the LSB comes first).

See Also

AP.PSIA.Tx.Data.PostPadType,
AP.PSIA.Tx.Data.PrePadType,
AP.PSIA.Rx.Data.MsbFirst

Example

See AP.PSIA.Rx.Data.EdgeSync.

AP.PSIA.Rx.Data.MSBFirst
AP.PSIA.Tx.Data.MSBFirst

Property

Syntax

AP.PSIA.Rx.Data.MSBFirst

AP.PSIA.Tx.Data.MSBFirst

Data Type

Boolean

True	MSB first
False	LSB first

Description

For the transmitter side (Tx), this command specifies whether audio data is sent Most Significant Bit (MSB) first or Least Significant Bit (LSB) first. For the receiver side (Rx), this command specifies whether audio data is accepted MSB first or LSB first.

See Also

AP.PSIA.Rx.Data.Justify

Example See AP.PSIA.Rx.Data.EdgeSync.

AP.PSIA.Rx.Data.PadBits
AP.PSIA.Tx.Data.PadBits

Property

Syntax **`AP.PSIA.Rx.Data.PadBits`**
`AP.PSIA.Tx.Data.PadBits`

Data Type Long — 0–24 (limited also by the number of bits per channel and the digital resolution)

Description For the transmitter side (Tx), this command sets the number of leading (leftmost) pad bits. If the sum of the number of pad bits and the number of bits in the audio word is less than the number of bits per channel, the subframe will also be padded with trailing bits. For the receiver side (Rx), this command sets the offset in bits of the audio data in the subframe, that is, the number of bits that will be skipped before audio data is clocked in.

See Also `AP.PSIA.Tx.Data.PostPadType`, `AP.PSIA.Tx.Data.PrePadType`, `AP.PSIA.Rx.BitClk.Factor`, `AP.S2CDio.InResolution`, `AP.S2CDio.OutResolution`

Example See AP.PSIA.Rx.Data.EdgeSync.

AP.PSIA.Rx.FrameClk.BitWidePulse
AP.PSIA.Tx.FrameClk.BitWidePulse

Property

Syntax **`AP.PSIA.Rx.FrameClk.BitWidePulse`**
`AP.PSIA.Tx.FrameClk.BitWidePulse`

Data Type Boolean

`True`	Bit-wide pulse (one period of the bit clock)
`False`	Approximately 50% duty cycle

Description

This command selects the pulse width of the frame clock output. Assuming that the frame clock output is not inverted, and not set to shift 1 bit left, the following are true:

- When FrameClk.BitWidePulse is *True*, the frame clock is high for the first bit of each frame, and low for the rest of the frame.
- When FrameClk.BitWidePulse is *False*, and the number of channels C is even, the frame clock is high for the first C/2 subframes, and low for the rest of the frame.
- When FrameClk.BitWidePulse is *False*, and the number of channels C is odd, the frame clock is high for the first (C-1)/2 subframes, and low for the rest of the frame.

Note: this command is not available when the associated frame clock direction is set to IN.

See Also

`AP.PSIA.Rx.FrameClk.Dir, AP.PSIA.Rx.FrameClk.Rate, AP.PSIA.Rx.FrameClk.EdgeSync, AP.PSIA.Rx.FrameClk.InvWfm, AP.PSIA.Rx.FrameClk.ShiftOneBitLeft`

Example

```
Sub Main
AP.PSIA.Tx.FrameClk.Dir = 0
                  ' output
  AP.PSIA.Tx.FrameClk.EdgeSync = 0
                  ' assert on bitclk rise
  AP.PSIA.Tx.FrameClk.InvWfm = True
                  ' invert
  AP.PSIA.Tx.FrameClk.ShiftOneBitLeft = True
                  ' shift one bit left
  AP.PSIA.Tx.FrameClk.BitWidePulse = False
                  ' 50% duty cycle
  AP.PSIA.Tx.FrameClk.Rate("Hz") = 44100
                  ' CD sample rate
  AP.PSIA.Rx.FrameClk.Dir = 1
                  ' input
  AP.PSIA.Rx.FrameClk.EdgeSync = 1
                  ' latch on bitclk fall
  AP.PSIA.Rx.FrameClk.InvWfm = True
                  ' inverted
```

```
    AP.PSIA.Rx.FrameClk.ShiftOneBitLeft  = True
                    ' shifted one bit left
    AP.PSIA.Rx.FrameClk.Rate("Hz") = 44100
                    ' CD sample rate
End Sub
```

AP.PSIA.Rx.FrameClk.Dir
AP.PSIA.Tx.FrameClk.Dir

Property

Syntax **AP.PSIA.Rx.FrameClk.Dir**
AP.PSIA.Tx.FrameClk.Dir

Data Type Integer

0	Output
1	Input

Description This command selects the frame clock direction. Each frame clock port can be configured as an output or as an input. In output (master) mode, the frame clock is provided by the PSIA. In input (slave) mode, the frame clock is provided by an external source.

See Also AP.PSIA.Rx.FrameClk.BitWidePulse, AP.PSIA.Rx.FrameClk.EdgeSync, AP.PSIA.Rx.FrameClk.InvWfm, AP.PSIA.Rx.FrameClk.Rate, AP.PSIA.Rx.FrameClk.ShiftOneBitLeft

Example See AP.PSIA.Rx.FrameClk.BitWidePulse.

AP.PSIA.Rx.FrameClk.EdgeSync
AP.PSIA.Tx.FrameClk.EdgeSync

Property

Syntax **AP.PSIA.Rx.FrameClk.EdgeSync**
AP.PSIA.Tx.FrameClk.EdgeSync

Data Type Integer

0	Rising edge
1	Falling edge

Description When the direction of the associated frame clock is set to OUT, this command selects whether the frame clock output is asserted at the rising or falling edge of the bit clock. When the direction of the associated frame clock is set to IN, this command selects whether the frame clock input is latched at the rising or falling edge of the bit clock.

See Also
`AP.PSIA.Rx.FrameClk.BitWidePulse`,
`AP.PSIA.Rx.FrameClk.Dir`,
`AP.PSIA.Rx.FrameClk.InvWfm`,
`AP.PSIA.Rx.FrameClk.Rate`,
`AP.PSIA.Rx.FrameClk.ShiftOneBitLeft`

Example See AP.PSIA.Rx.FrameClk.BitWidePulse.

AP.PSIA.Rx.FrameClk.InvWfm
AP.PSIA.Tx.FrameClk.InvWfm

Property

Syntax
`AP.PSIA.Rx.FrameClk.InvWfm`
`AP.PSIA.Tx.FrameClk.InvWfm`

Data Type Boolean

`True`	Inverted frame clock
`False`	Non-inverted frame clock

Description This command sets the polarity of the frame clock. When set to *False* (non-inverted), the frame clock is high at the start of the frame, and low for the rest of the frame. When set to *True* (inverted), the frame clock is low at the start of the frame, and high for the rest of the frame.

See Also
`AP.PSIA.Rx.FrameClk.BitWidePulse`,
`AP.PSIA.Rx.FrameClk.Dir`,
`AP.PSIA.Rx.FrameClk.EdgeSync`,
`AP.PSIA.Rx.FrameClk.Rate`,
`AP.PSIA.Rx.FrameClk.ShiftOneBitLeft`

Example See AP.PSIA.Rx.FrameClk.BitWidePulse.

AP.PSIA.Rx.FrameClk.Rate
AP.PSIA.Tx.FrameClk.Rate

Property

Syntax

AP.PSIA.Rx.FrameClk.Rate(ByVal *Unit* As String**)**

AP.PSIA.Tx.FrameClk.Rate(ByVal *Unit* As String**)**

Data Type Double

Parameter

Name	Description
Unit	The following unit is available: Hz

Description When the direction of the associated frame clock is set to OUT, FrameClk.Rate sets the frequency of the frame clock output in Hz. Typically this is equal to the sample rate of the digital audio stream. When the direction of the associated frame clock is set to IN, FrameClk.Rate is used only to compute the displayed rates in the 'computed rate' column on the PSIA panels.

See Also AP.PSIA.Rx.FrameClk.BitWidePulse, AP.PSIA.Rx.FrameClk.Dir, AP.PSIA.Rx.FrameClk.EdgeSync, AP.PSIA.Rx.FrameClk.InvWfm, AP.PSIA.Rx.FrameClk.ShiftOneBitLeft

Example See AP.PSIA.Rx.FrameClk.BitWidePulse.

AP.PSIA.Rx.FrameClk.ShiftOneBitLeft
AP.PSIA.Tx.FrameClk.ShiftOneBitLeft

Property

Syntax

AP.PSIA.Rx.FrameClk.ShiftOneBitLeft

AP.PSIA.Tx.FrameClk.ShiftOneBitLeft

Data Type Boolean

True	Frame clock valid one bit time before start of frame
False	Frame clock valid at start of frame

Description This command allows the frame clock to be asserted (when associated frame clock direction is OUT) or latched (when associated frame clock direction is IN) one bit time before the actual start of the frame. Typically, this is used in the I^2S bus standard. When

FrameClk.ShiftOneBitLeft is *False*, the frame clock is asserted or latched at the start of the frame. When FrameClk.ShiftOneBitLeft is *True*, the frame clock is asserted or latched one bit time before the start of the frame.

See Also `AP.PSIA.Rx.FrameClk.BitWidePulse`, `AP.PSIA.Rx.FrameClk.Dir`, `AP.PSIA.Rx.FrameClk.EdgeSync`, `AP.PSIA.Rx.FrameClk.InvWfm`, `AP.PSIA.Rx.FrameClk.Rate`

Example See AP.PSIA.Rx.FrameClk.BitWidePulse.

AP.PSIA.Rx.I2S
AP.PSIA.Tx.I2S

Method

Syntax **`AP.PSIA.Rx.I2S`**
`AP.PSIA.Tx.I2S`

Description This command configures the transmitter or receiver settings to be compatible with the Philips I^2S (Inter-IC Sound) bus.

See Also `AP.PSIA.Rx.FrameClk.ShiftOneBitLeft`

Example

```
Sub Main
     AP.PSIA.Tx.I2S ' I2S output format
     AP.PSIA.Tx.LoopBack ' copy settings to receiver
End Sub
```

AP.PSIA.Rx.MasterClk.Factor
AP.PSIA.Tx.MasterClk.Factor

Property

Syntax **`AP.PSIA.Rx.MasterClk.Factor`**
`AP.PSIA.Tx.MasterClk.Factor`

Data Type Long 1 or more

Description This command specifies the ratio (factor) between the master clock and the frame clock. Depending on other clock settings, certain factors may not be achievable.

Note: this command is not available when the associated master clock direction is set to OUT.

See Also `AP.PSIA.MasterClkDir`

Example See AP.PSIA.MasterClkDir, AP.PSIA.Rx.NFsClk.Factor.

AP.PSIA.Rx.NFsClk.Factor
AP.PSIA.Tx.NFsClk.Factor

Property

Syntax **`AP.PSIA.Rx.NFsClk.Factor`**
`AP.PSIA.Tx.NFsClk.Factor`

Data Type Long 1 or more

Description This command specifies the ratio (factor) between the N*Fs clock and the frame clock. Depending on other clock settings, certain factors may not be achievable.

See Also `AP.PSIA.Rx.NFsClk.InvWfm`

Example See AP.PSIA.MasterClkDir.

AP.PSIA.Rx.NFsClk.InvWfm
AP.PSIA.Tx.NFsClk.InvWfm

Property

Syntax **`AP.PSIA.Rx.NFsClk.InvWfm`**
`AP.PSIA.Tx.NFsClk.InvWfm`

Data Type Boolean

`True`	Inverted N*Fs clock
`False`	Non-inverted N*Fs clock

Description This command sets the polarity of the N*Fs clock. When set to *False* (non-inverted), the N*Fs clock is high at the start of the frame, and low

for the rest of the frame. When set to *True* (inverted), the N*Fs clock is low at the start of the frame, and high for the rest of the frame.

See Also `AP.PSIA.Rx.NFsClk.Factor`

Example See AP.PSIA.MasterClkDir.

AP.PSIA.Tx.BitClk.Dir — Property

See `AP.PSIA.Rx.BitClk.Dir`

AP.PSIA.Tx.BitClk.Factor — Property

See `AP.PSIA.Rx.BitClk.Factor`

AP.PSIA.Tx.ChannelClk.BitWidePulse — Property

See `AP.PSIA.Rx.ChannelClk.BitWidePulse`

AP.PSIA.Tx.ChannelClk.EdgeSync — Property

See `AP.PSIA.Rx.ChannelClk.EdgeSync`

AP.PSIA.Tx.ChannelClk.Factor — Property

See `AP.PSIA.Rx.ChannelClk.Factor`

AP.PSIA.Tx.ChannelClk.InvWfm — Property

See `AP.PSIA.Rx.ChannelClk.InvWfm`

AP.PSIA.Tx.Data.ChannelA

Property

See AP.PSIA.Rx.Data.ChannelA

AP.PSIA.Tx.Data.ChannelB

Property

See AP.PSIA.Rx.Data.ChannelB

AP.PSIA.Tx.Data.EdgeSync

Property

See AP.PSIA.Rx.Data.EdgeSync

AP.PSIA.Tx.Data.Justify

Method

See AP.PSIA.Rx.Data.Justify

AP.PSIA.Tx.Data.MSBFirst

Property

See AP.PSIA.Rx.Data.MSBFirst

AP.PSIA.Tx.Data.PadBits

Property

See AP.PSIA.Rx.Data.PadBits

AP.PSIA.Tx.Data.PostPadType

Property

Syntax **AP.PSIA.Tx.Data.PostPadType**

Data Type Integer

0	Low: Set post (trailing) padding bits to logical low
1	High: Set post (trailing) padding bits to logical high

2	First bit: Set post (trailing) padding bits to the state of the last bit of the audio word

Description This command selects the value of the pad bits that trail the audio word. All pad bits have the same value: logical low, logical high, or the same state as the last bit in the audio word. In a two's complement coding scheme, the MSB is the sign bit.
Therefore if the audio word is ordered LSB first, and AP.PSIA.Tx.Data.PostPadType = 2, then the audio word will be sign extended by the trailing pad bits.

See Also `AP.PSIA.Tx.Data.PrePadType`, `AP.PSIA.Rx.Data.PadBits`

Example See AP.PSIA.Rx.Data.EdgeSync.

AP.PSIA.Tx.Data.PrePadType — Property

Syntax **`AP.PSIA.Tx.Data.PrePadType`**

Data Type Integer

0	Low: Set pre (leading) padding bits to logical low
1	High: Set pre (leading) padding bits to logical high
2	First bit: Set pre (leading) padding bits to the state of the first bit of the audio word

Description This command selects the value of the pad bits that lead the audio word. All pad bits have the same value: logical low, logical high, or the same state as the first bit in the audio word. In a two's complement coding scheme, the MSB is the sign bit.
Therefore if the audio word is ordered MSB first, and AP.PSIA.Tx.Data.PrePadType = 2, then the audio word will be sign extended by the leading pad bits.

See Also `AP.PSIA.Tx.Data.PostPadType`, `AP.PSIA.Rx.Data.PadBits`

Example See AP.PSIA.Rx.Data.EdgeSync.

AP.PSIA.Tx.FrameClk.BitWidePulse

Property

See AP.PSIA.Rx.FrameClk.BitWidePulse

AP.PSIA.Tx.FrameClk.Dir

Property

See AP.PSIA.Rx.FrameClk.Dir

AP.PSIA.Tx.FrameClk.EdgeSync

Property

See AP.PSIA.Rx.FrameClk.EdgeSync

AP.PSIA.Tx.FrameClk.InvWfm

Property

See AP.PSIA.Rx.FrameClk.InvWfm

AP.PSIA.Tx.FrameClk.Rate

Property

See AP.PSIA.Rx.FrameClk.Rate

AP.PSIA.Tx.FrameClk.ShiftOneBitLeft

Property

See AP.PSIA.Rx.FrameClk.ShiftOneBitLeft

AP.PSIA.Tx.I2S

Method

See AP.PSIA.Rx.I2S

AP.PSIA.Tx.LoopBack

Method

Syntax **`AP.PSIA.Tx.LoopBack`**

Description This command configures the receiver according to the current transmitter settings, to provide a way to check data integrity through the PSIA. The following external connections are required to complete the loopback configuration (BNC-BNC cables are supplied for this purpose):

Transmitter bit clock → receiver bit clock

Transmitter frame clock → receiver frame clock

Transmitter data → receiver data

Example See AP.PSIA.Rx.I2S.

AP.PSIA.Tx.MasterClk.Factor

Property

See `AP.PSIA.Rx.MasterClk.Factor`

AP.PSIA.Tx.NFsClk.Factor

Property

See `AP.PSIA.Rx.NFsClk.Factor`

AP.PSIA.Tx.NFsClk.InvWfm

Property

See `AP.PSIA.Rx.NFsClk.InvWfm`

AP.PSIA.VoltageSetting

Property

Syntax **`AP.PSIA.VoltageSetting`**

Data Type Constant

`PSIA_1_8_CMOS` 1.8 V CMOS

PSIA_2_4_CMOS	2.4 V CMOS
PSIA_3_3_CMOS	3.3 V CMOS
PSIA_3_3_TTL	3.3 V TTL
PSIA_5_TTL	5.0 V TTL

Description This command sets the input and output voltages according to the logic family and voltage supplied.

Note: the outputs must be on for signal to appear at the PSIA outputs.

See Also `AP.PSIA.OutputsOn`

Example See AP.PSIA.MasterClkDir.

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